System Design Guide for IN/OUT Slave

Motor Business Unit
Appliances Company

Revision History

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Revision	Date	Change Description
1	2006/6/30	Initial Release
2	2007/6/4	P5 Added output reset at timeout. Minor edits.
3	2012/2/20	P1 Changed title from “Reference Circuit Diagram for IN/OUT Module”. Integrated “Overview of the Protocol for IN/OUT Module Rev2”. P3 Added introduction. P6 Added applicable PHY. P8 Added ESD protection. P9 Corrected communication state. P11 Added timing chart. Minor edits.

Introduction

This document is to describe an example of system design for the IN/OUT slave.

Modes of ASIC MNM1221:

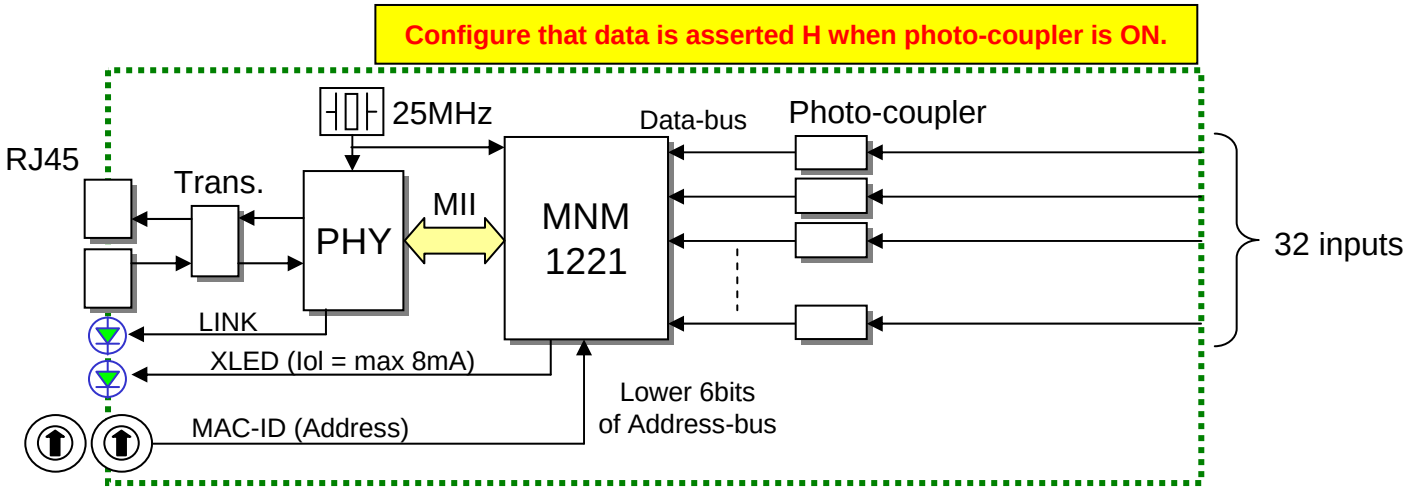
	Master	Slave	
		Generic (Note)	IN / OUT
CPU	Need	Need	No Need
Data Pins	Data Bus (32 or 16bit)	Data Bus (16 or 8bit)	Input or Output Pins (32)
Address Pins	Address Bus	Address Bus	MAC-ID Setting
Pin91	XWAIT	XWAIT	XLED
Trigger of Transmitting	Internal Timer or XTXTIM input	Receiving Frame	Receiving Frame
XSYNC Output Timing	Transmitting	After All Slaves Receiving (RUNNING State Only)	After All Slaves Receiving (RUNNING State Only)
Conditions of Timeout Detection	No Receiving before the Next Transmitting	No Receiving for a Certain Time Set with Register	No Receiving for a Certain Time (20.9ms Fixed)

Note: "Generic" mode can be used for various applications also including in/out device.

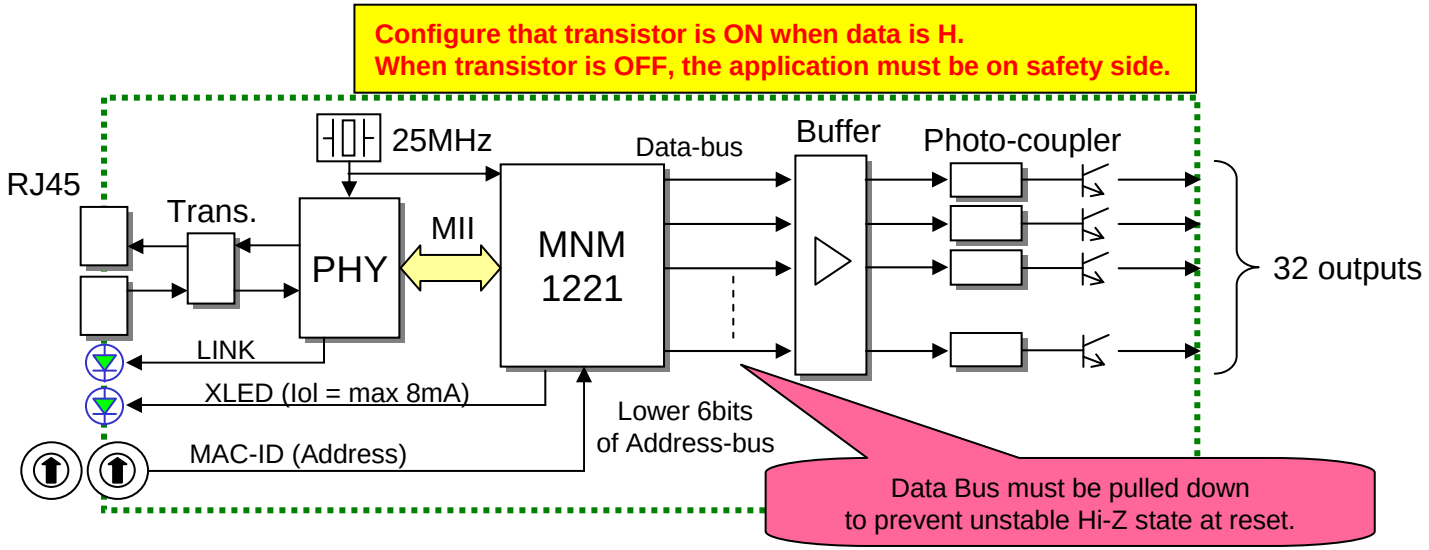
System Structure

Block Diagram

IN



OUT



Applicable PHY

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For PHY, either BCM5221 or DP83848 must be used.
KSZ8041 cannot be used for I/O slave because it needs to set internal MII registers.

	Broadcom BCM5221KPTG	NS DP83848I	Micrel KSZ8041MLLI
Package	QFP64 10 x 10mm	QFP48 7 x 7mm	QFP48 7 x 7mm
Supply Voltage	3.0 to 3.6V	3.0 to 3.6V	3.14 to 3.47V
Operating Ambient Temp.	-40 to +85 deg C	-40 to +85 deg C	-40 to +85 deg C
RoHS Compliant	Yes	Yes	Yes
Limitation of PHY Address	None	Do not use address 0.	Do not use address 0.
MII Register Setting	No need	No need	Needed
In I/O slave without CPU	Applicable	Applicable	Do not use

MNM1221 Mode Setting

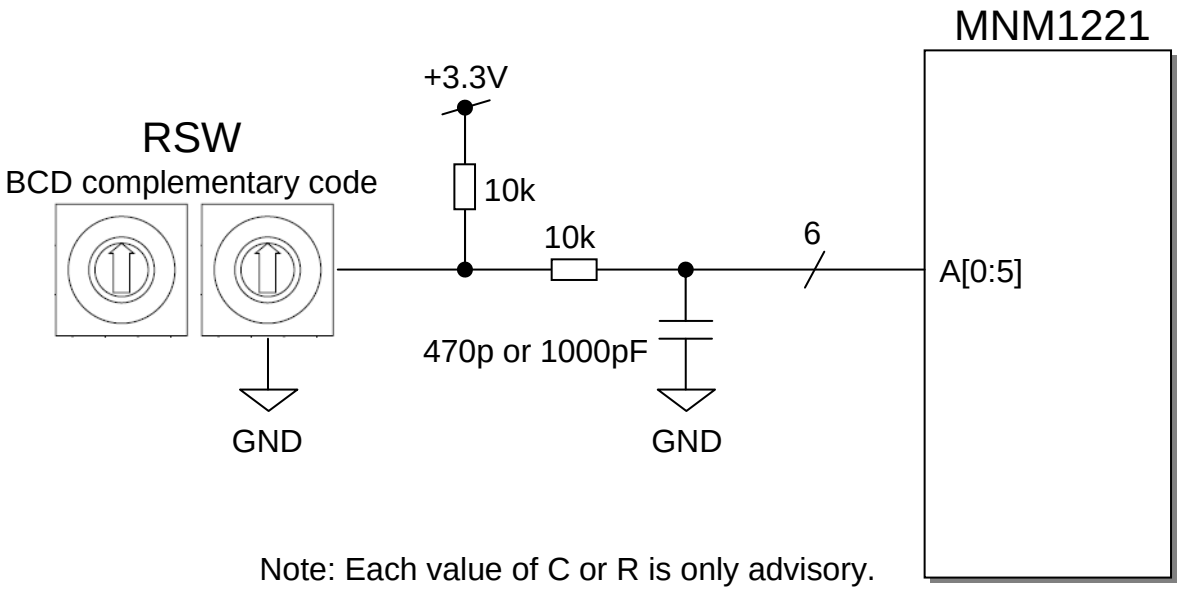
MODE1 (pin59)	MODE0 (pin58)	BUSMODE (pin60)	Mode	Valid Data-bus as input or output	Valid Address-bus as MAC-ID
1	0	0	32ch IN Slave	D0 to D31	A0 to A4 BIN
		1			A0 to A5 BCD
	1	0	32ch OUT Slave	D0 to D31	A0 to A3 BIN
		1			A0 to A5 BCD

Unused pin should be pulled down with 10k Ohm.

Unused pin must be tied to GND.

ESD Protection

Between address setting RSW and MNM1221,
low-pass filters to prevent ESD must be installed.



Note: Each value of C or R is only advisory.

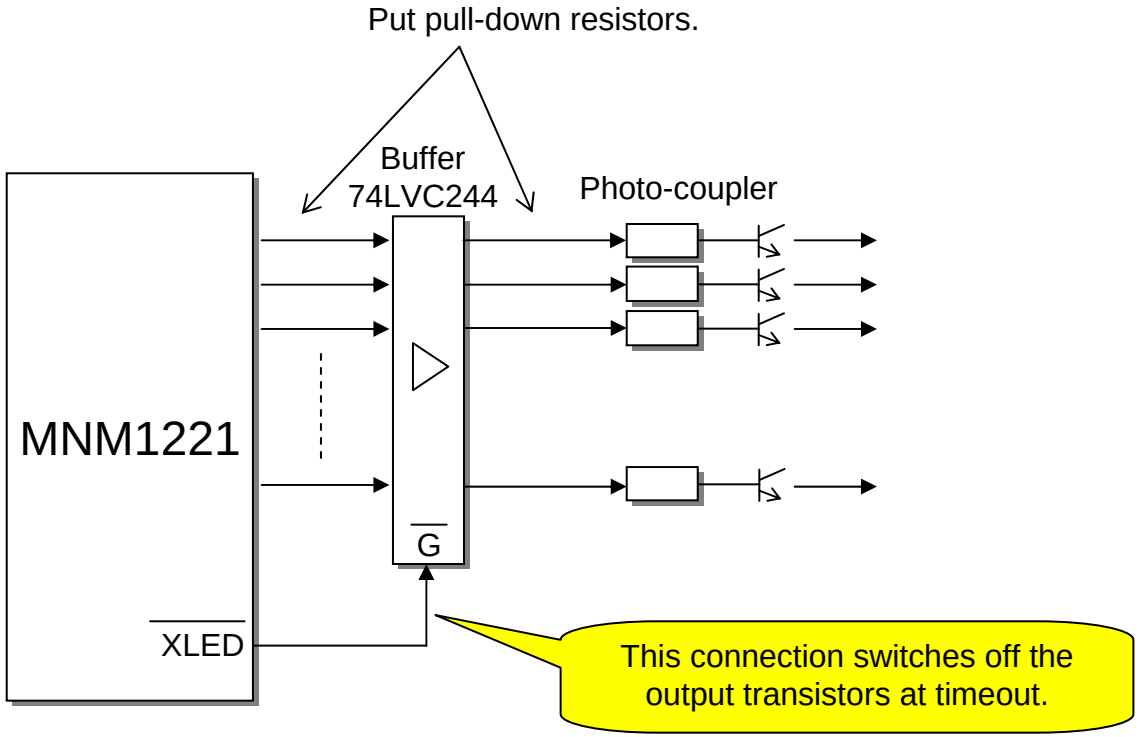
LED Output from MNM1221

Communication State		LED	Remark
INITIAL CONFIG-A CONFIG-B		Disappear	
RUNNING	Normal Operation	**Green**	**“RUNNING state” and “Not Timeout”**
	Timeout	Disappear	Detection Time: 20.8896ms

Notes:
- MNM1221 does not have a detection of “Continuous CRC Error”. So, in this case, LED is Green.
- In output-module, if CRC Error is detected, output is not updated and previous OK data is held.
- In output-module, if Timeout is detected, output is held with the latest data.

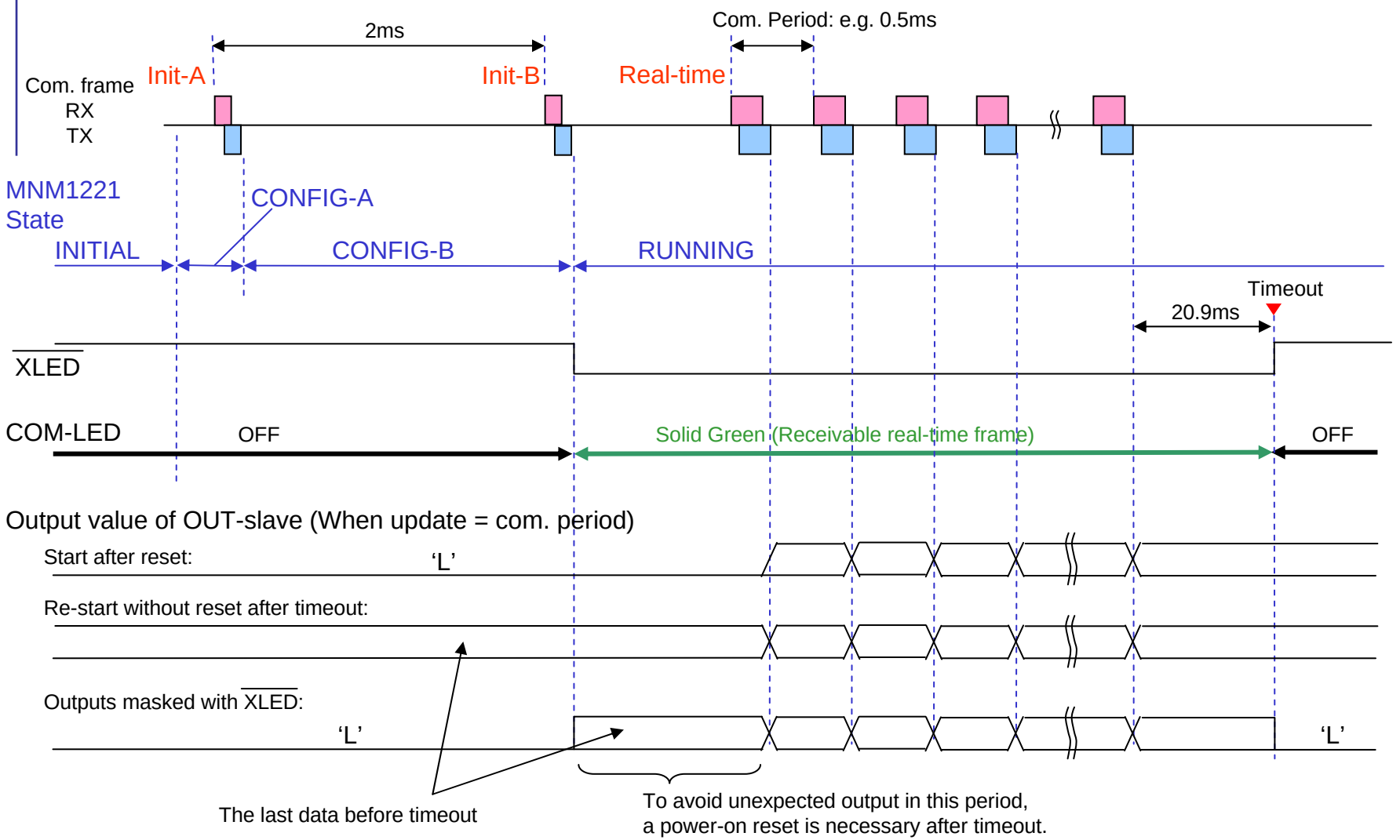
Output Reset at Timeout

Output module keeps previous output level after timeout.
If output transistors must be switched off for safety,
the following circuit diagram should be designed.



After timeout, turn off power and confirm whether communication cables has any problems.

Timing Chart



Timing

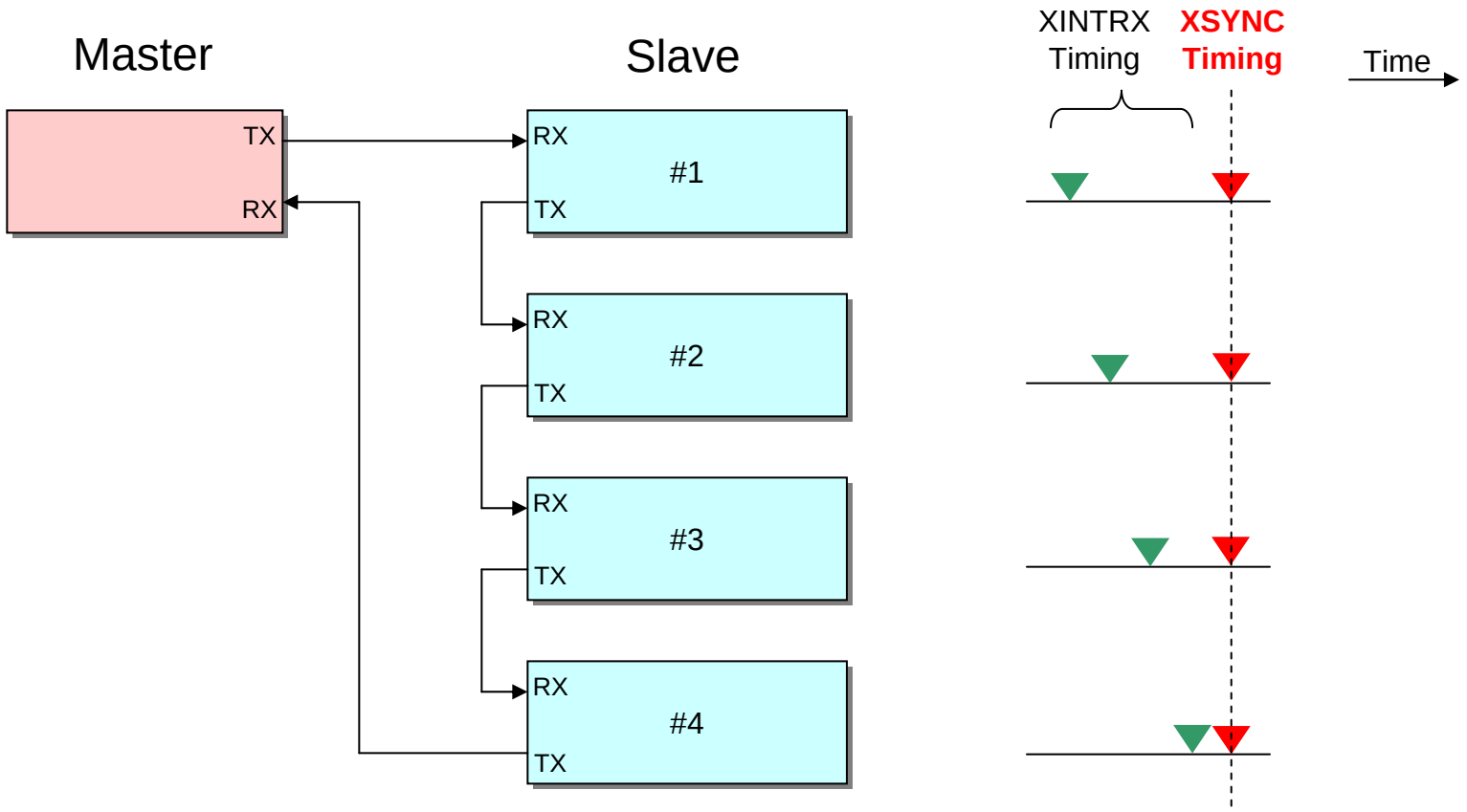
Reflection of IN/OUT Data

In both IN and OUT module, data is sampled or outputted at falling edge of XSYNC of MNM1221.

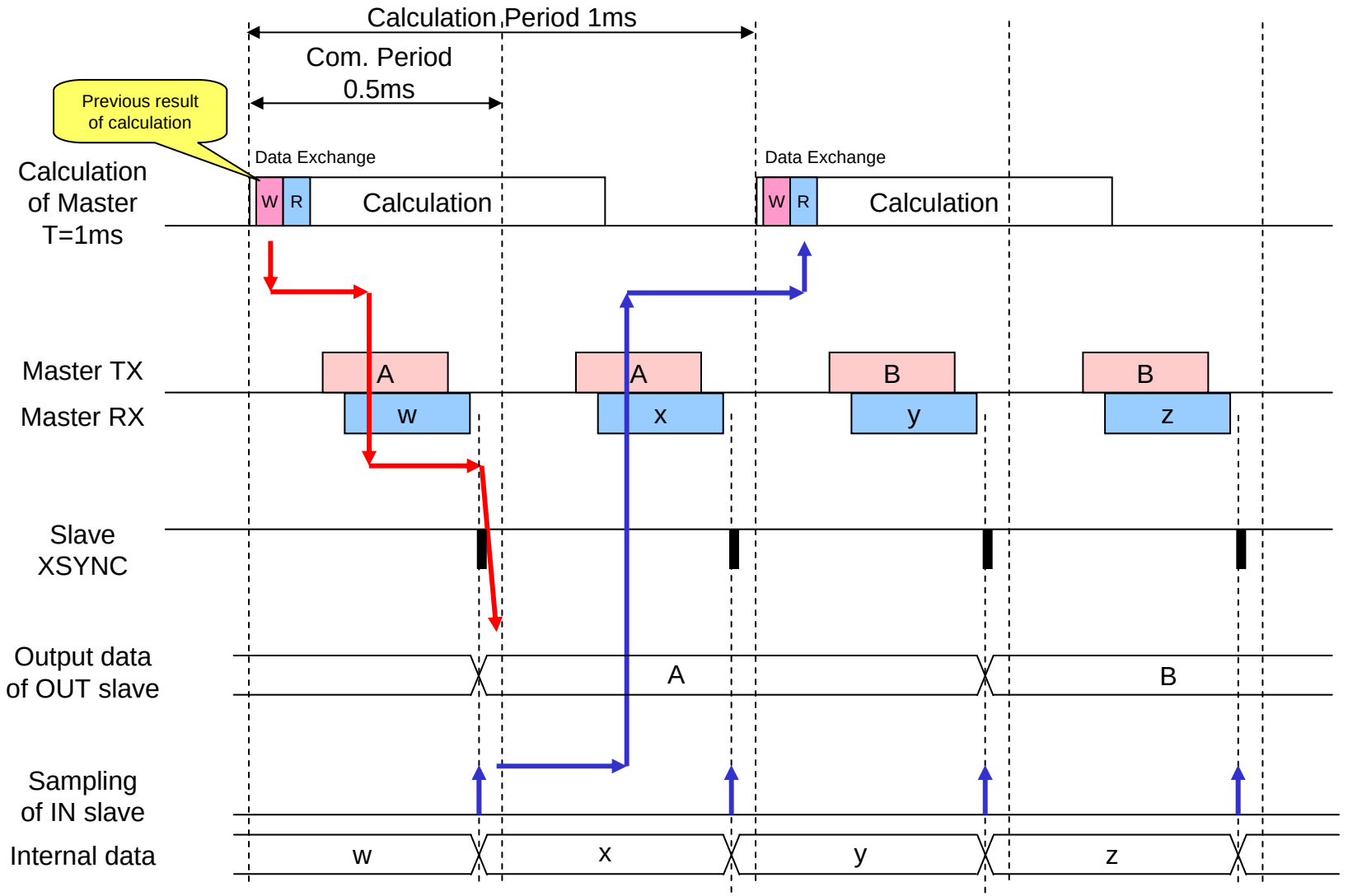
	IN	OUT
Data Reflection Timing	Data is sampled at XSYNC timing, and replied to Master in the next period.	RX data is outputted at XSYNC timing.
Reset and After reset	RX data is zero(0) before the first sampling.	Zero(0) is outputted before the first RX.

XSYNC Output Timing

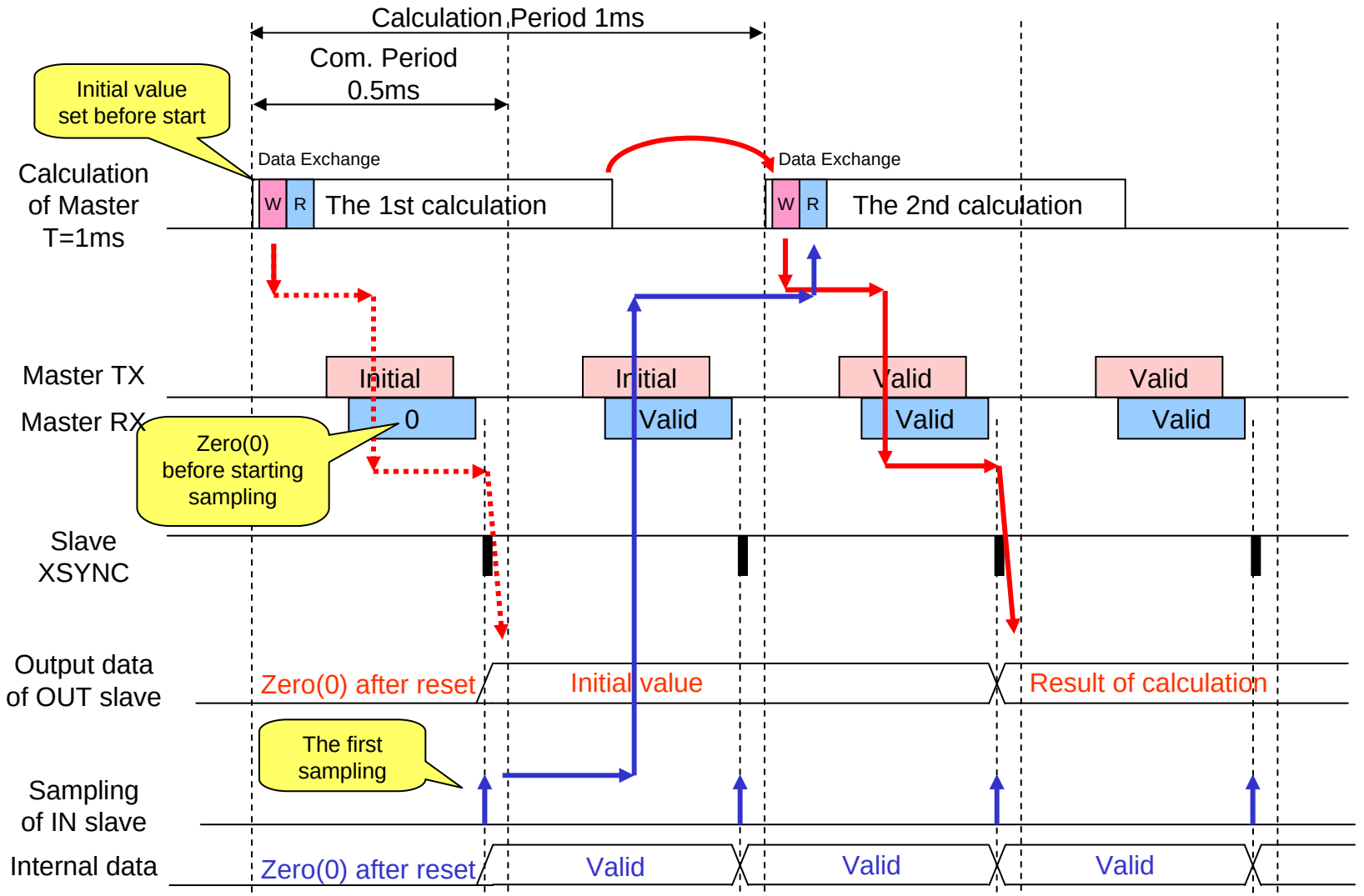
At the same time, XSYNCs of all slaves are outputted.



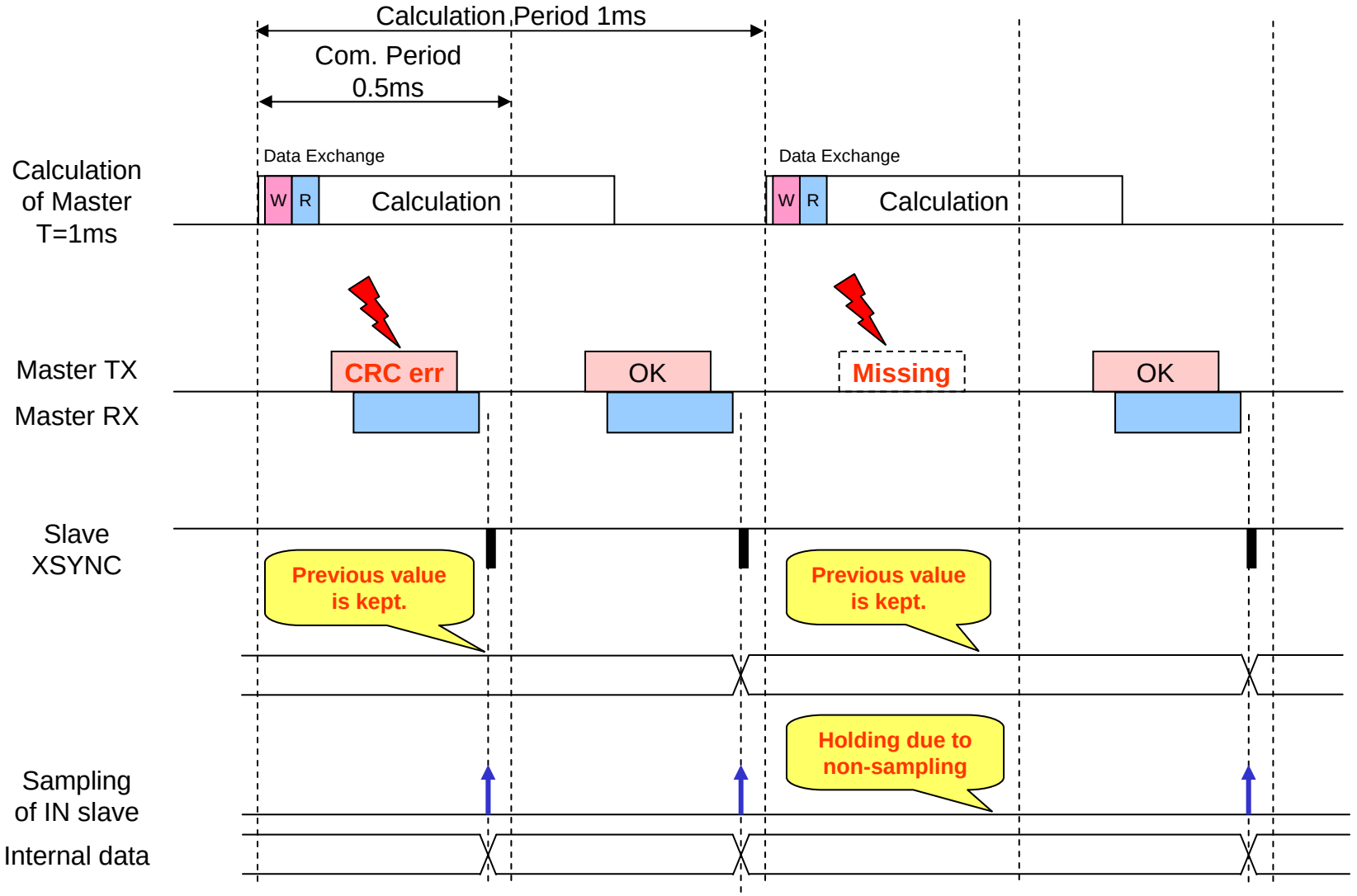
Timing of Data Transmission



Timing at Start-up

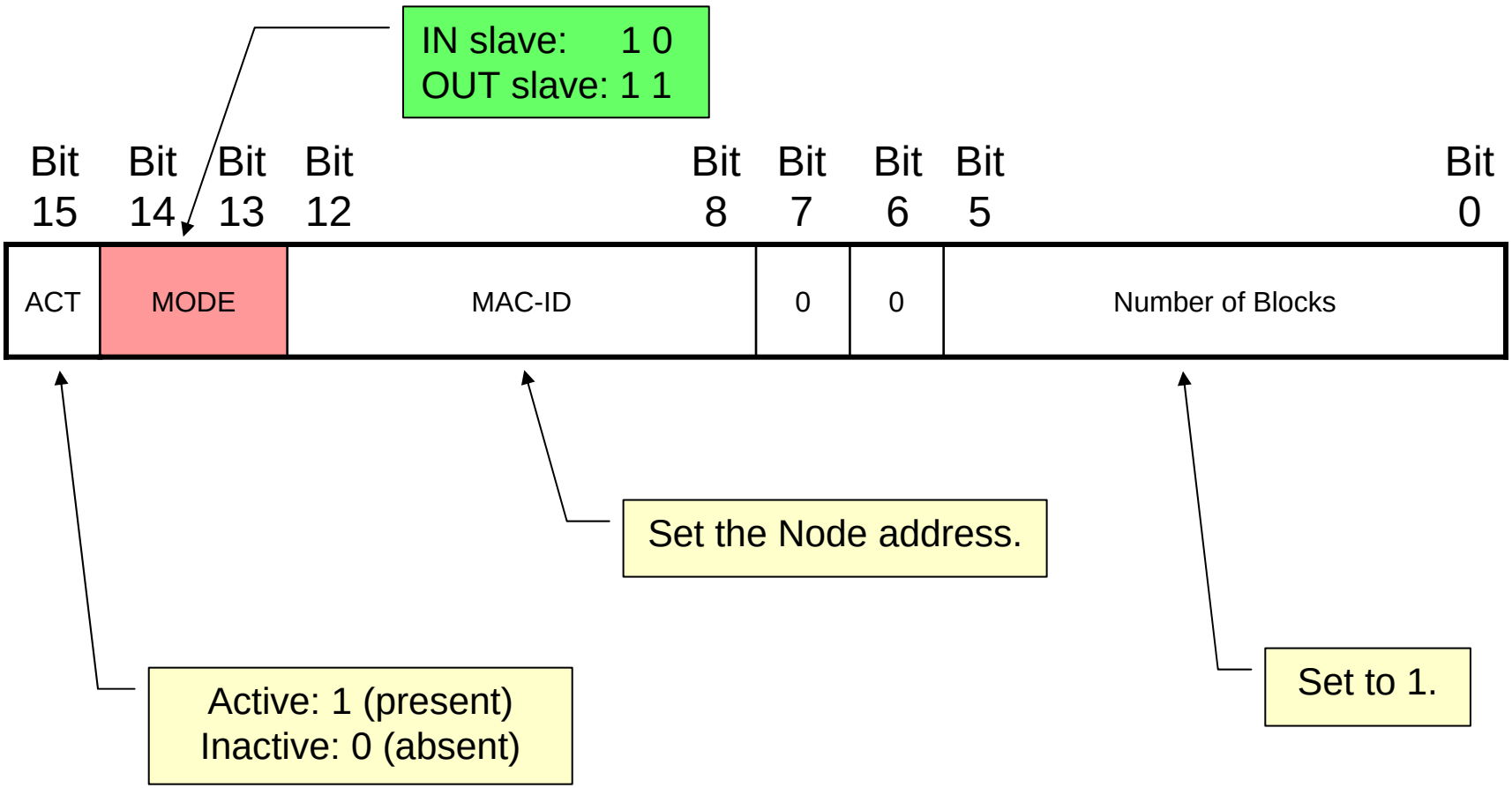


Timing at Communication Error



Slave Information Table

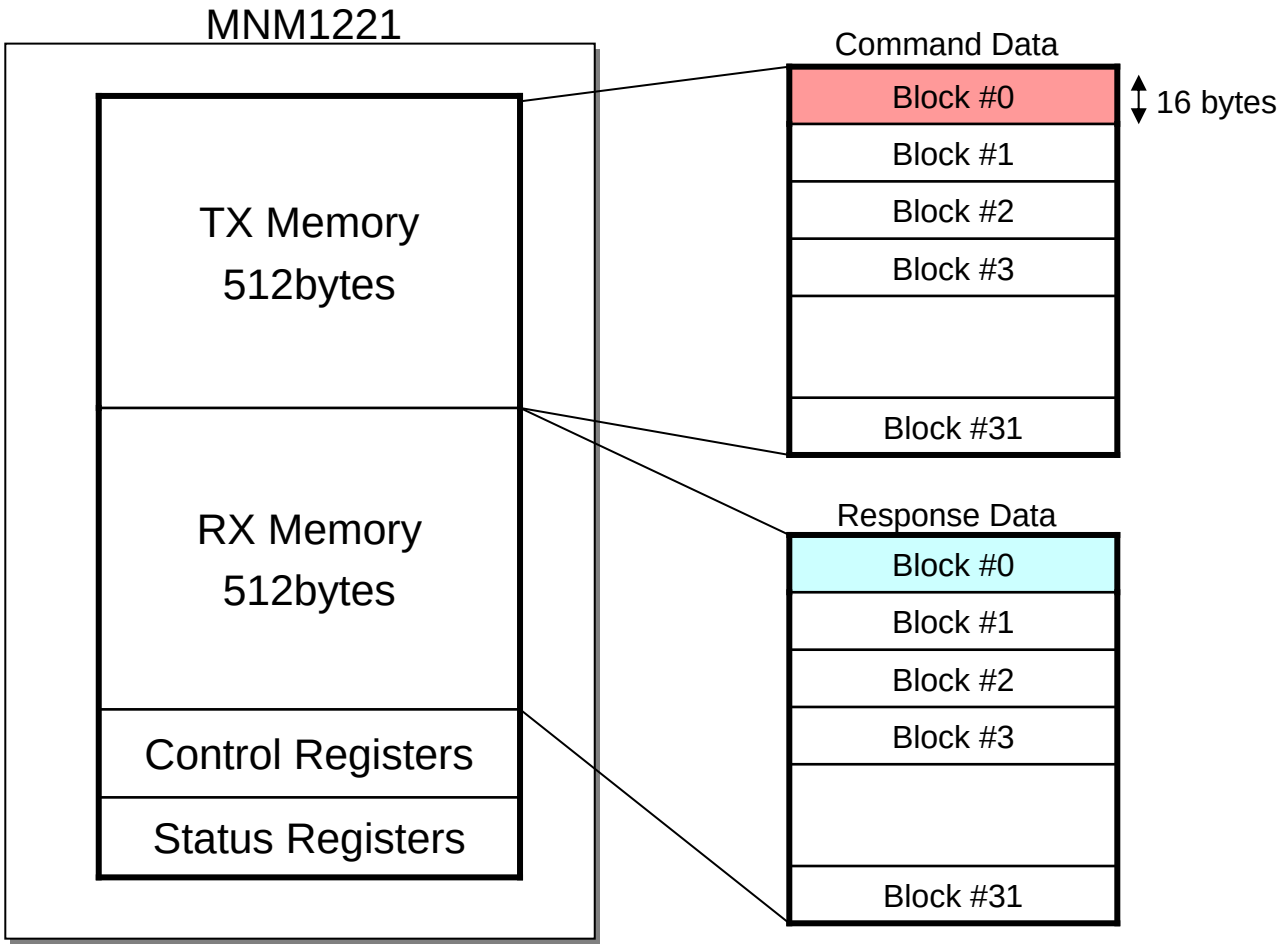
Slave Information Table Setup



Data Block for TX & RX

Occupied Block

An IN/OUT module occupies one data block (16bytes).



TX & RX for I/O Slave

In the communication with I/O slave, byte4 to 7 in the data block is used. Update Counter and MAC-ID should be written like a servo. Though they are not used in the I/O slave and not reflected in the response, they helps analysis when trouble.

IN module

Input data is byte4 to 7 in the response.
- 0: input photo-coupler is OFF
- 1: input photo-coupler is ON

The first received data is not actual input, but invalid zero(0) data.
So do not use it for the control.

OUT module

Byte4 to 7 written in the command is outputted.
- 0: output transistor is OFF
- 1: output transistor is ON

In the initial state from power-ON to the first data receiving of OUT module, zero(0) is outputted. Therefore, when 0 is outputted, the system must be on safety side.

Command (Controller to I/O)

Write the C/R, Update Counter and MAC-ID for easy analysis of trouble.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte0	C/R (0)	Update Counter			MAC-ID (0 to 31)			
Byte1	0	0						
Byte2	0	0	0	0	0	0	0	0
Byte3	0	0	0	0	0	0	0	0
Byte4	OUT slave: Output data IN slave: Zero(0) data							
Byte5								
Byte6								
Byte7								
Byte8	0							
Byte9								
Byte10								
Byte11								
Byte12	0							
Byte13								
Byte14								
Byte15								

Note: Data is in order of “little endian”, i.e. lower-byte first.

Response (I/O to Controller)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Byte0								
Byte1								
Byte2								
Byte3								
Byte4	IN slave: Input data OUT slave: Indefinite							
Byte5								
Byte6								
Byte7								
Byte8	IN slave: Indefinite OUT slave: Previous output data							
Byte9								
Byte10								
Byte11								
Byte12								
Byte13								
Byte14								
Byte15								

Note1: Data in non-color area is indefinite.
Note2: Data is in order of “little endian”, i.e. lower-byte first.

IN Slave

Command

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
byte0	0	Update Counter		MAC-ID				
byte1	0							
byte2								
byte3								
byte4	0							
byte5								
byte6								
byte7								
byte8	0							
byte9								
byteA								
byteB								
byteC	0							
byteD								
byteE								
byteF								

Response

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Not Used							
D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8
D23	D22	D21	D20	D19	D18	D17	D16
D31	D30	D29	D28	D27	D26	D25	D24
Not Used							
Not Used							

OUT Slave

Command

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
byte0	0	Update Counter		MAC-ID				
byte1	0							
byte2								
byte3								
byte4	D7	D6	D5	D4	D3	D2	D1	D0
byte5	D15	D14	D13	D12	D11	D10	D9	D8
byte6	D23	D22	D21	D20	D19	D18	D17	D16
byte7	D31	D30	D29	D28	D27	D26	D25	D24
byte8	0							
byte9								
byteA								
byteB								
byteC	0							
byteD								
byteE								
byteF								

Response

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Not Used							
Not Used							
B7	B6	B5	B4	B3	B2	B1	B0
B15	B14	B13	B12	B11	B10	B9	B8
B23	B22	B21	B20	B19	B18	B17	B16
B31	B30	B29	B28	B27	B26	B25	B24
Not Used							

Previous output value (echo back)