System Design Guide for Slave

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Revision History

Revision	Date	Change Description
1	2010/3/3	Initial Release
2	2012/2/15	P1 Changed title from “A Guide to Firmware Development for Slave”. P3 Added introduction. P5 Clarified the block diagram. Deleted MNM1221 block diagram. P7 Added XSYNC output timing. P9 Changed from SH7065F to SH7216 example. P10 Deleted XINTRX signal connection. P14 Added bus connection. P35 Added occupied blocks. Minor edits.

Introduction

This document is to describe an example of system design for the generic slave.

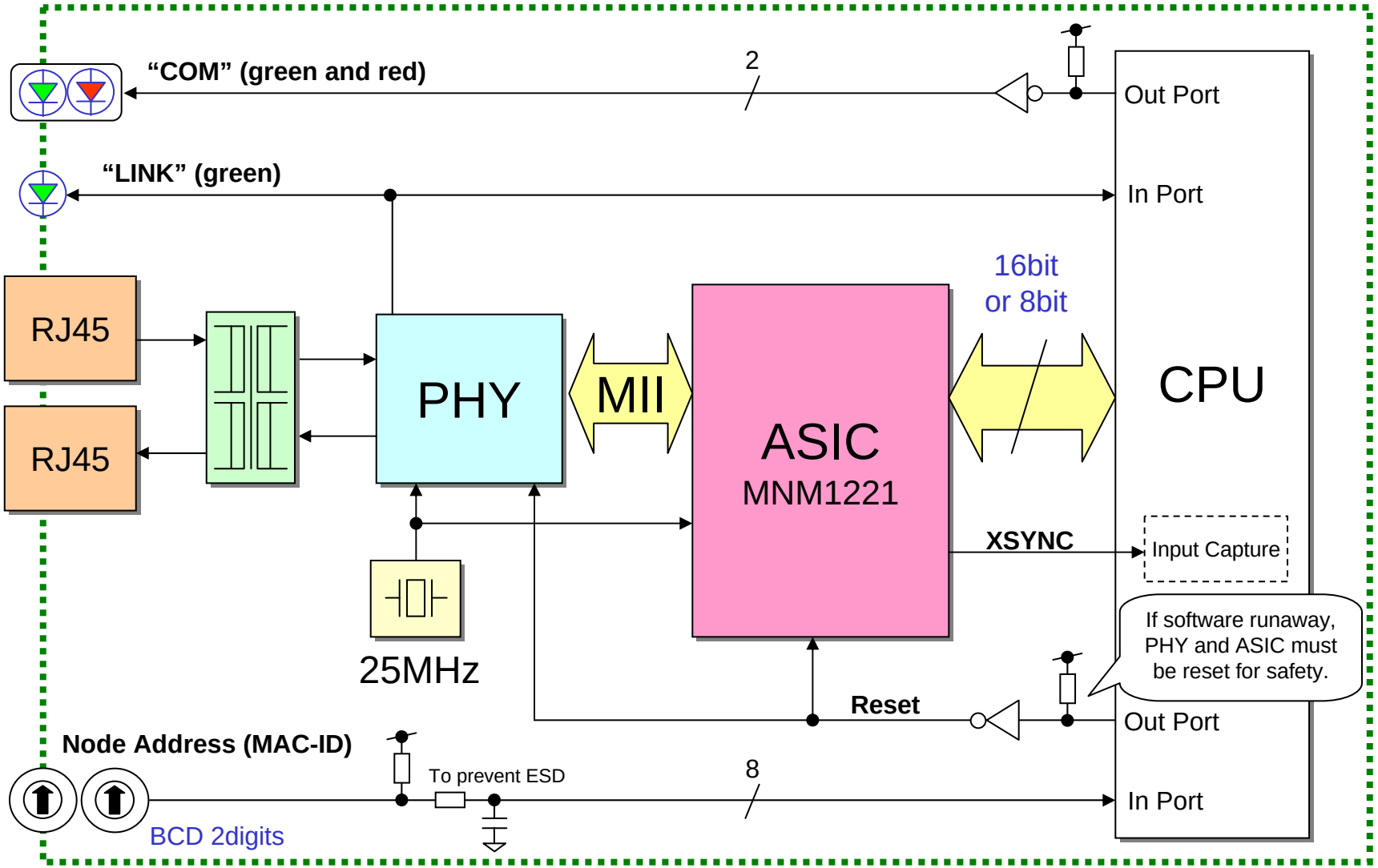
Modes of ASIC MNM1221:

	Master	Slave	
		Generic (Note)	**IN / OUT**
CPU	Need	Need	No Need
Data Pins	Data Bus (32 or 16bit)	Data Bus (16 or 8bit)	Input or Output Pins (32)
Address Pins	Address Bus	Address Bus	MAC-ID Setting
Pin91	XWAIT	XWAIT	XLED
Trigger of Transmitting	Internal Timer or XTXTIM input	Receiving Frame	Receiving Frame
XSYNC Output Timing	Transmitting	After All Slaves Receiving (RUNNING State Only)	After All Slaves Receiving (RUNNING State Only)
Conditions of Timeout Detection	No Receiving before the Next Transmitting	No Receiving for a Certain Time Set with Register	No Receiving for a Certain Time (20.9ms Fixed)

Note: "Generic" mode can be used for various applications also including in/out device.

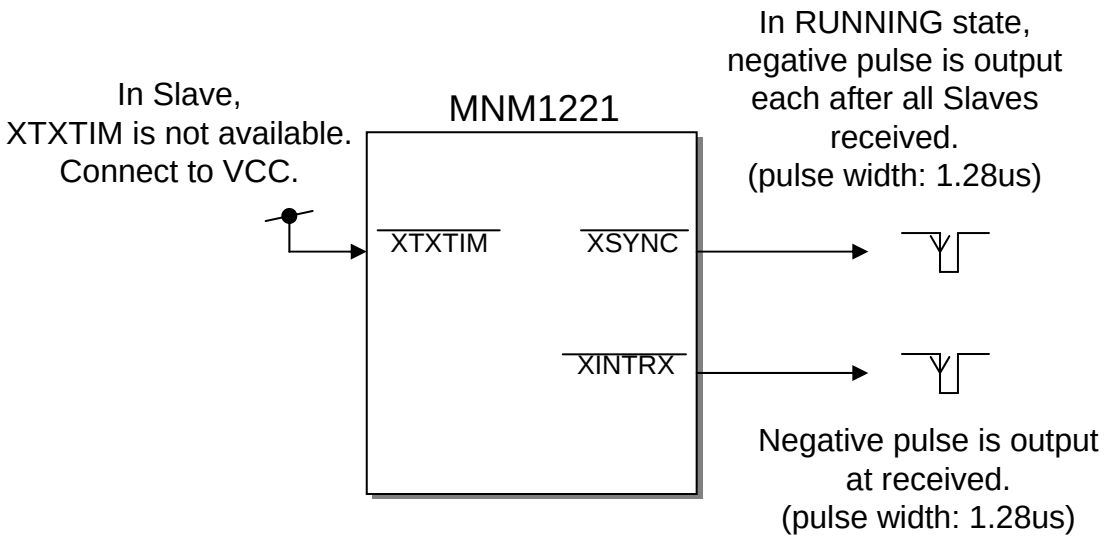
System Structure

Block Diagram for RTEX Circuit



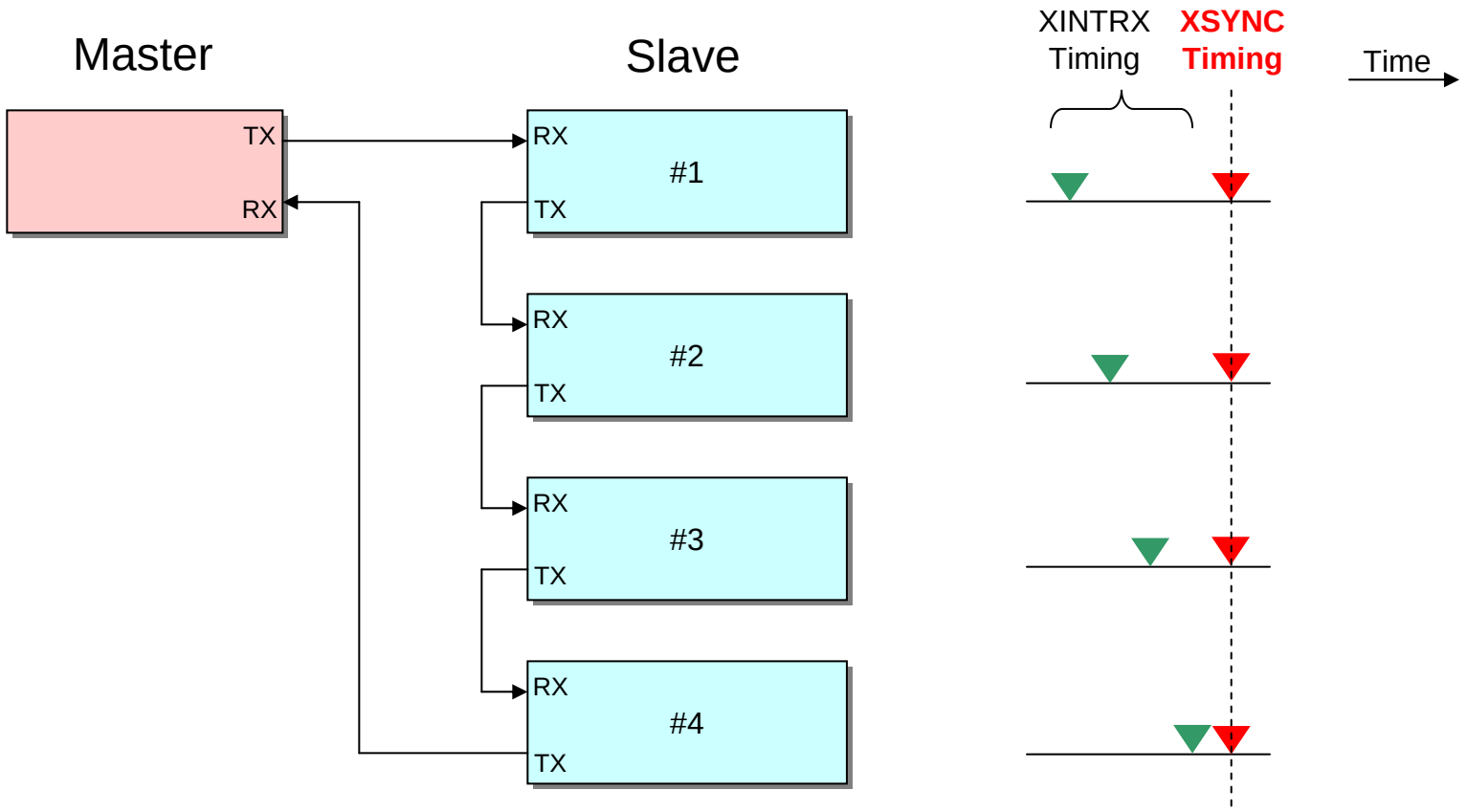
Timing Signals of MNM1221

In Slave, XSYNC is output at the same time after all Slaves received the frame. Synchronizing the calculation with this signal, all Slaves simultaneity is realized.



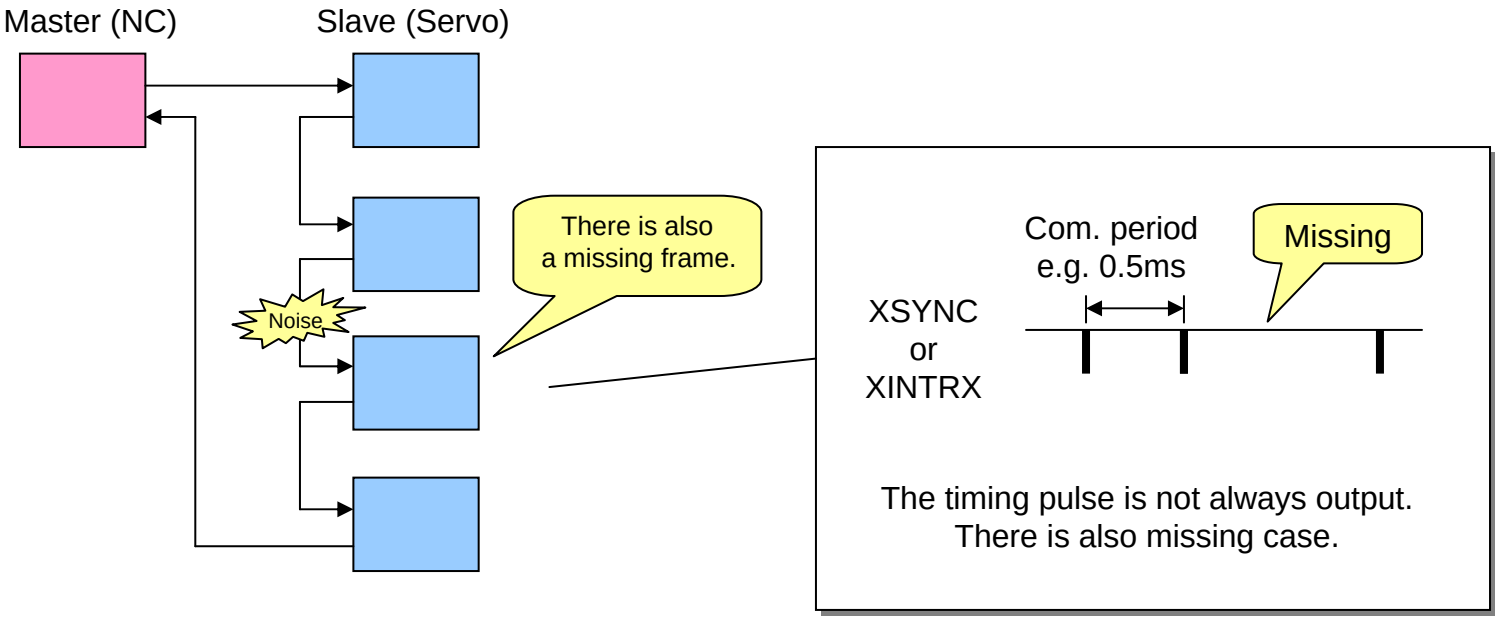
XSYNC Output Timing

At the same time, XSYNCs of all slaves are outputted.



Consideration for Com. Error

In communication error, there is a case where the frame is stopped as well as CRC error. In this case, since the frame cannot be received, XSYNC and XINTRX pulse are not output.



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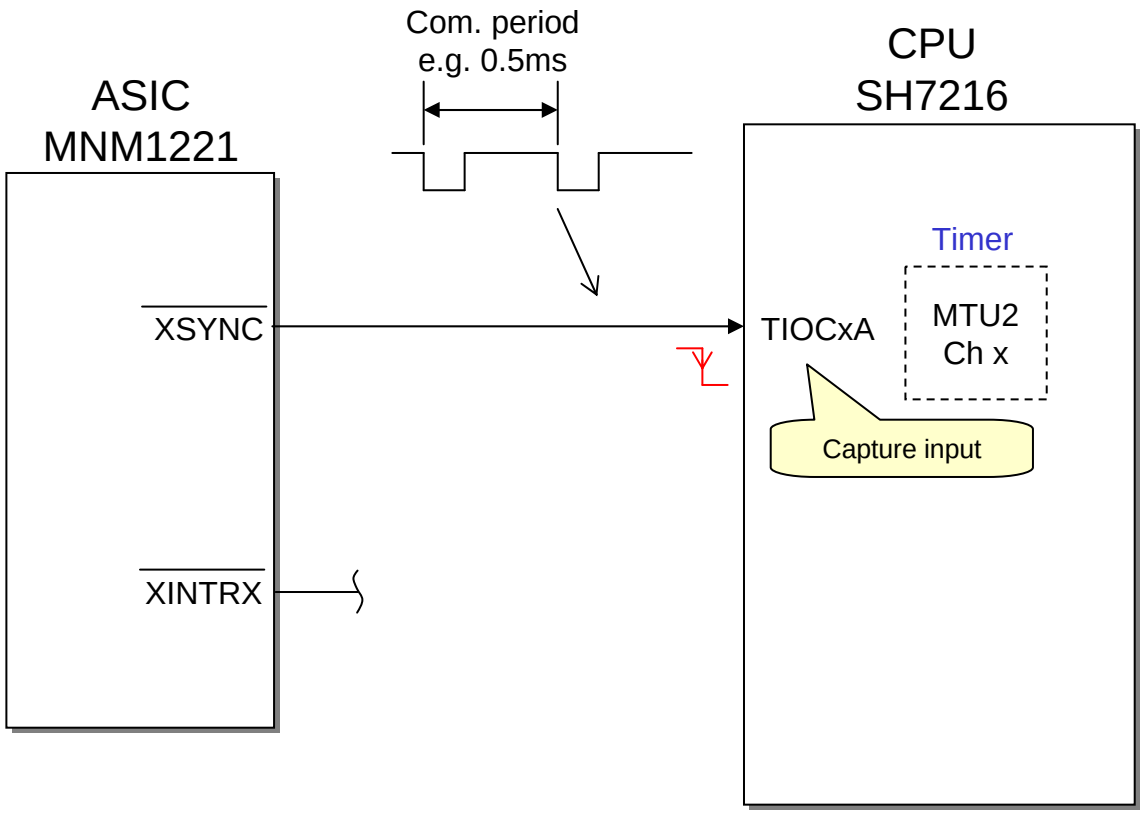
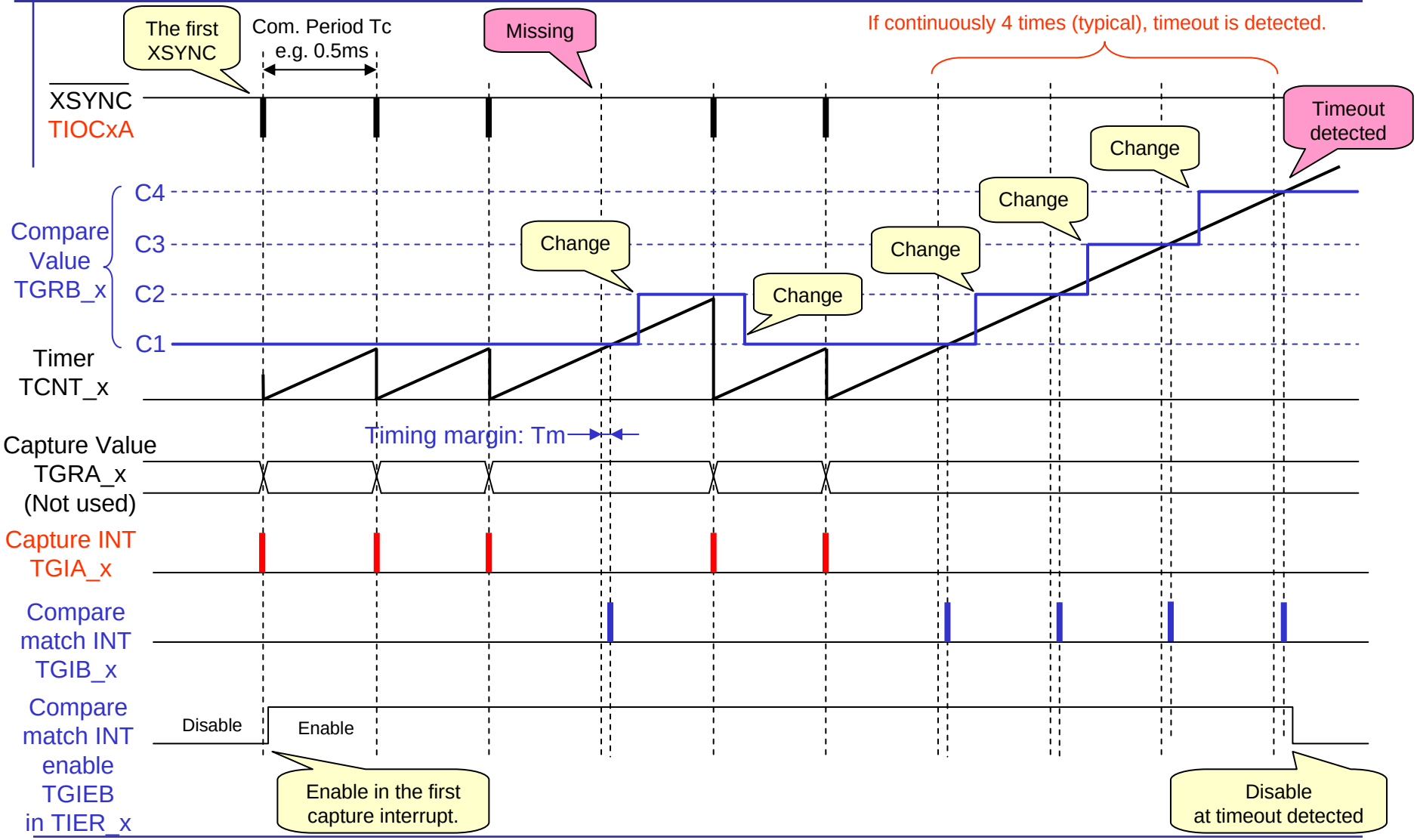
Example for SH7216 (Renesas)

Timing Signal Connection



- Connect XSYNC to a capture input of a timer in the CPU.
- At the falling edge, the timer is cleared and the interrupt occurs.

Timing Chart



Interrupt Setting

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During normal receiving, the input capture interrupt is used.
If missing, the compare match interrupt works.

Signal	Interrupt	Period	Trigger	Interrupt Enabling
TGIA_x	MTU2 Input Capture	e.g. 0.5ms	Normal receiving	Always enable.
TGIB_x	MTU2 Compare Match	e.g. 0.5ms	Frame missing	At the first XSYNC, enable in the capture INT. At timeout detected, disable.

Notes:
- If the frame missing, the previous data is used for the control. This way is the same as CRC error detected. If the data is command position, previous difference of position is used with assuming velocity is constant.
- The input capture is used for clearing the timer at interrupt occurrence, and TGRA_x capture value is not used.
- Because XSYNC is output in only RUNNING state, in the time from reset-released to the RUNNING state the process should be done by main loop.

Setting Compare Value

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To prevent both capture and compare-mach INT in normal receiving, the compare-mach INT timing must be delayed a little.
Therefore set as follows:

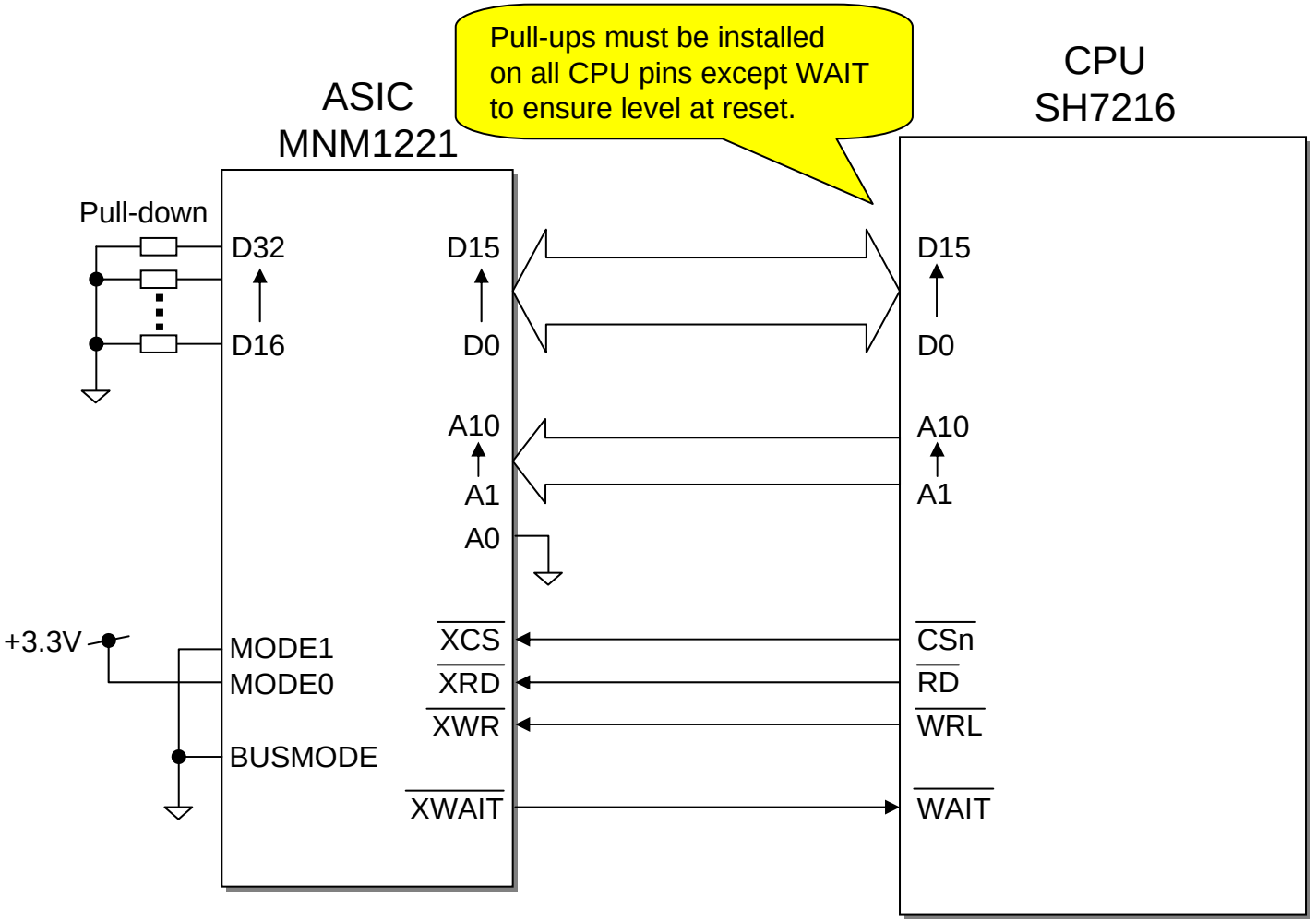
	Setting Value
C1	Tc + Tm
C2	2Tc + Tm
C3	3Tc + Tm
C4	4Tc + Tm

Tc: Communication Period
Tm: Timing Margin
(Set the larger value than the jitter of XSYNC.)

According to receiving situation, set TGRB_x to the following compare value.

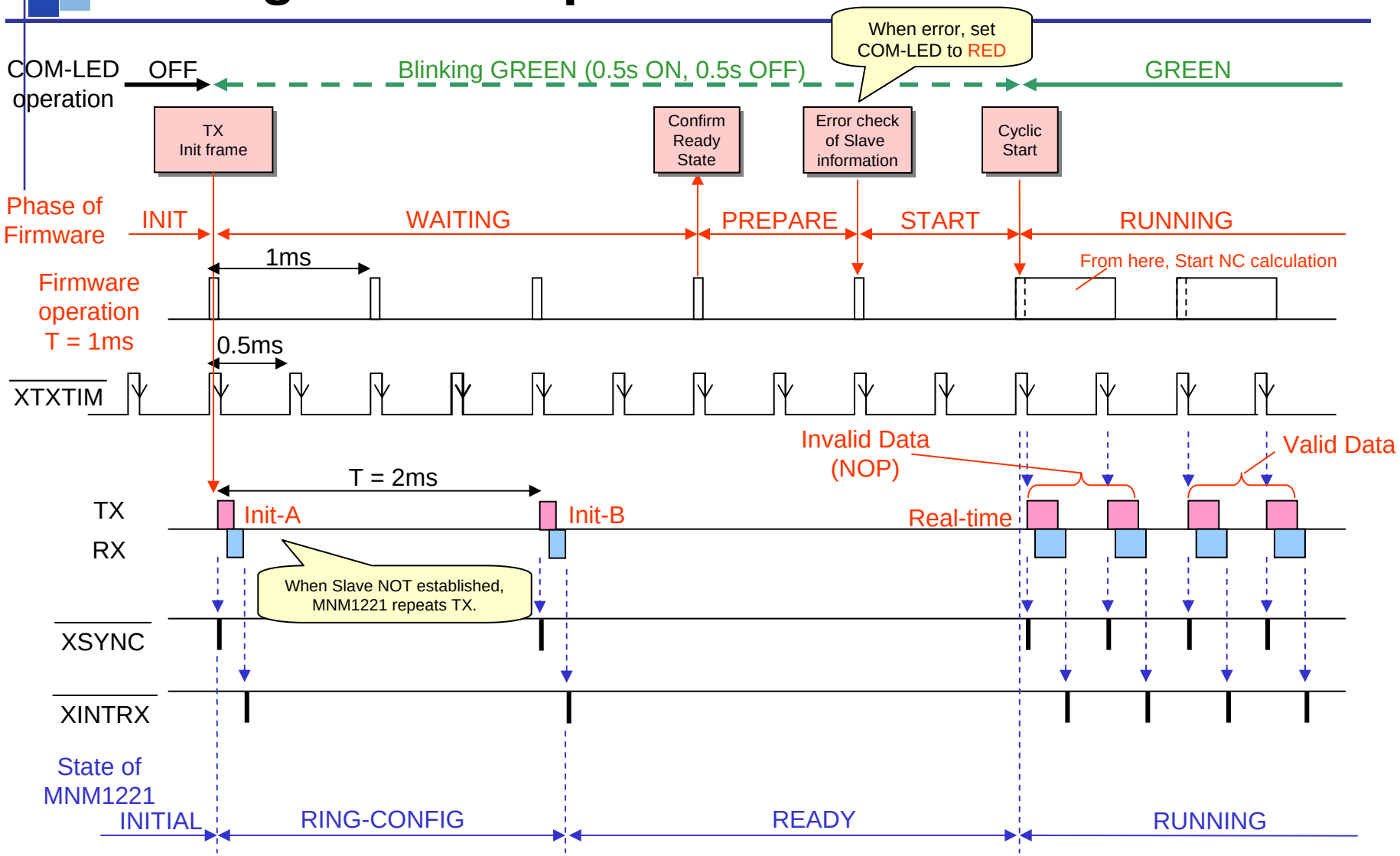
In capture INT	In compare-match INT
Set C1 (Initialize)	Each time interrupt, increment the compare value such as from C1 to C2.

Bus Connection

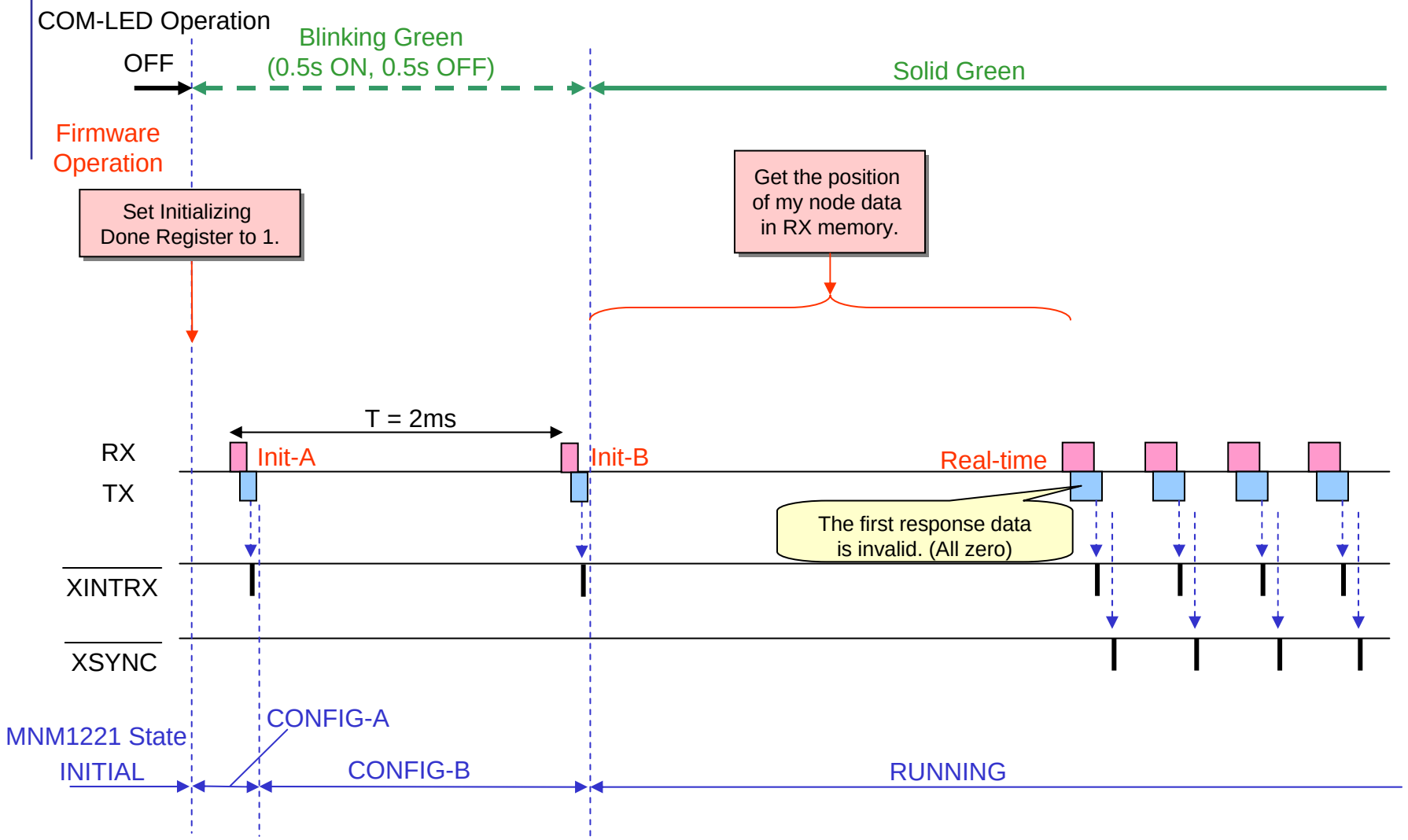


Timing Chart at Start-up

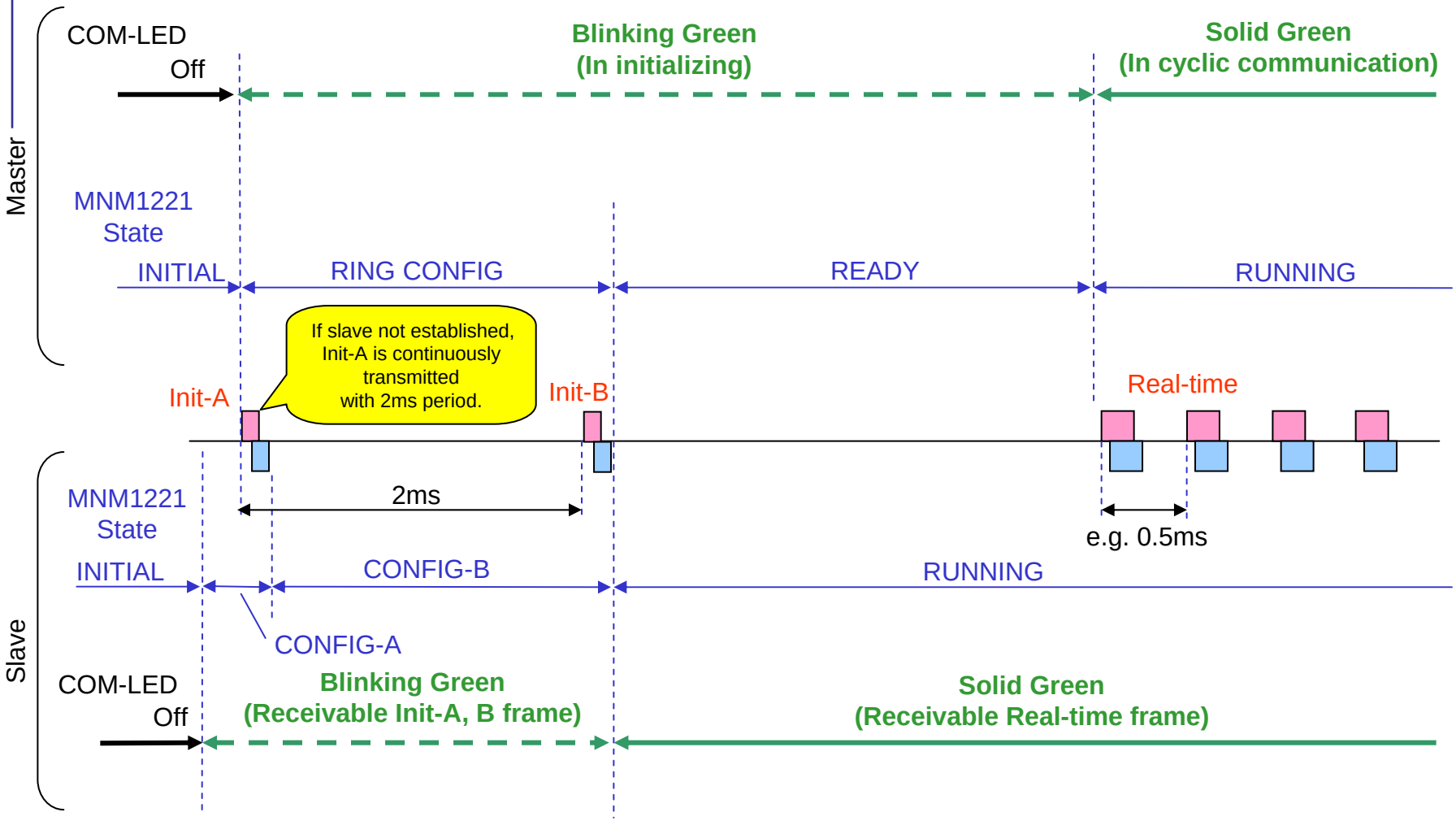
Timing at Start-up in Master



Timing at Start-up in Slave



State-Transition at Start-up



Example Code

Contents of Example Code

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The example code has basic functions for slave. The received data is moved into RX buffer in RAM, and TX buffer data is transmitted. An application program using this TX/RX buffer is assumed.

Files:

Name	Description
mnm1221_s.h	Header File
mnm1221_s.c	Source File

Functions:

Name	Placing	Description
init_mnm1221_s()	After Releasing Reset	Initializing
get_state_mnm1221_s()	Main Loop	Reading MNM1221 state
int_sync_mnm1221_s()	Interrupt by XSYNC	Com. Data Exchange
timeout_mnm1221_s()	At Timeout Detected	Operation at Timeout

Variables:

Name	Placing	Description
my_rx_buf[]	CPU internal RAM	RX Buffer
my_tx_buf[]	CPU internal RAM	TX Buffer

Programming by Yourself

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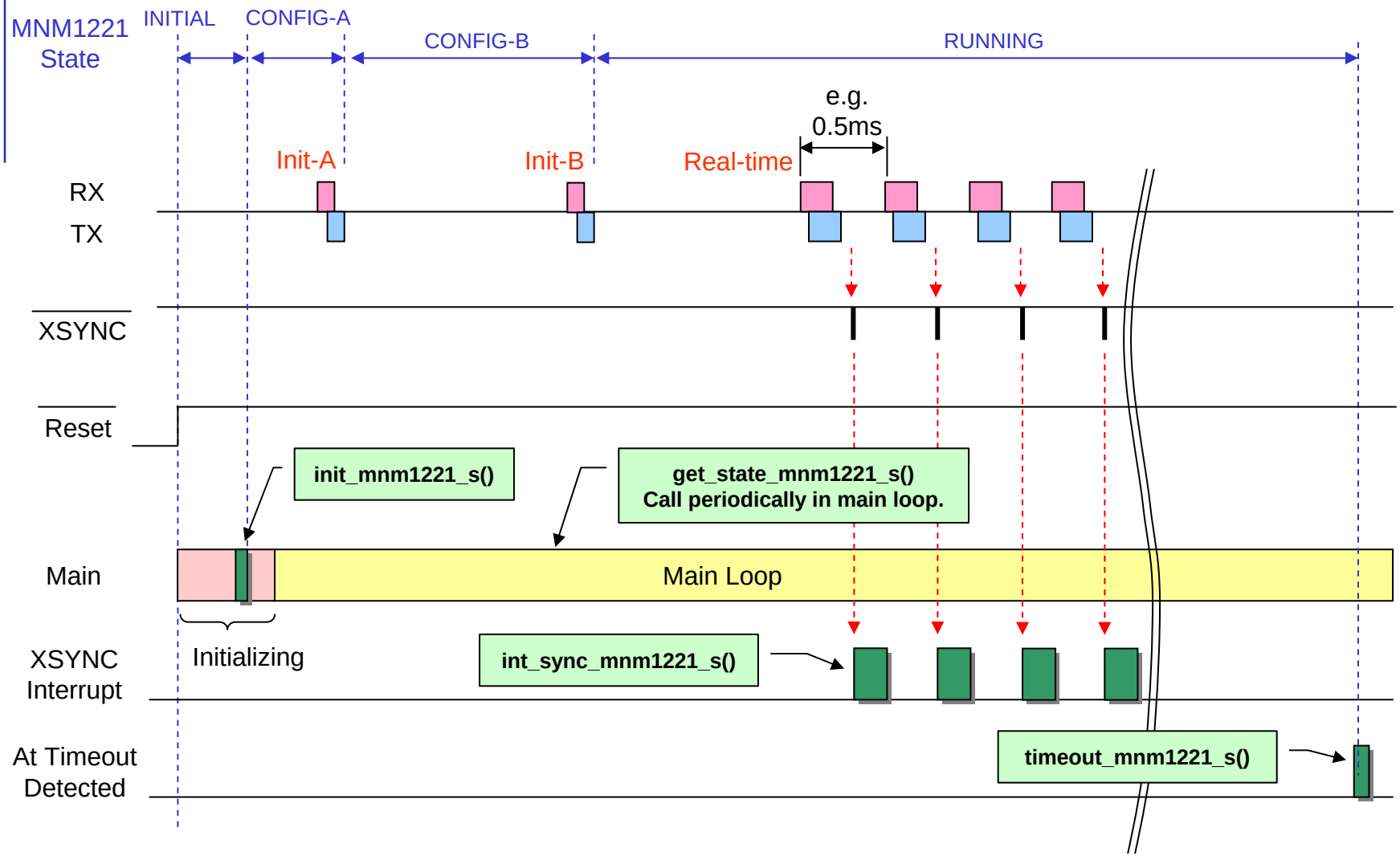
The followings are not included in the example code.

	Description	Remark
Application	Depend on your device.	Including detection of command error.
Reading MAC-ID	Reading rotary SW at power-on	Converting BCD to BIN. Error detection for out of setting range.
“COM” LED Operation	According to MNM1221 state and error, control LED.	2 Colors LED (Green / Red)
Timeout Detection	In RUNNING state, continuously not received.	e.g. Cable breaking down
Continuous CRC Error Detection	In RUNNING state, continuously CRC error detected.	If necessary, added for safety. In motion control, mandatory.

Note:
When the larger value is set to timeout detection or continuous CRC error detection, noise immunity is improved.
However, there is a trade-off that the detection time becomes longer and it might cause problem for safety.
After careful consideration, set suitable value for application. If error detected, it is necessary to control for safe side such as motion stop.

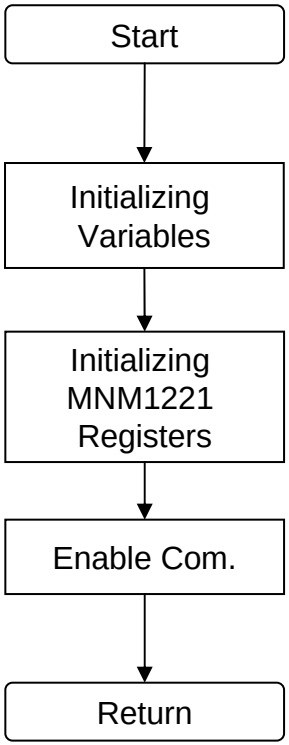
Location of Example Code



Flow Chart

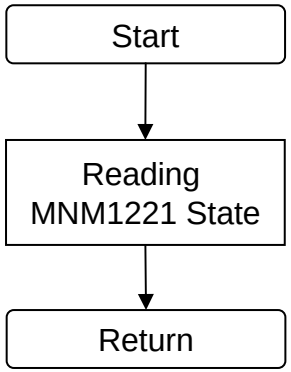
Initializing

Name	Description
init_mnm1221_s()	Initializing after Reset



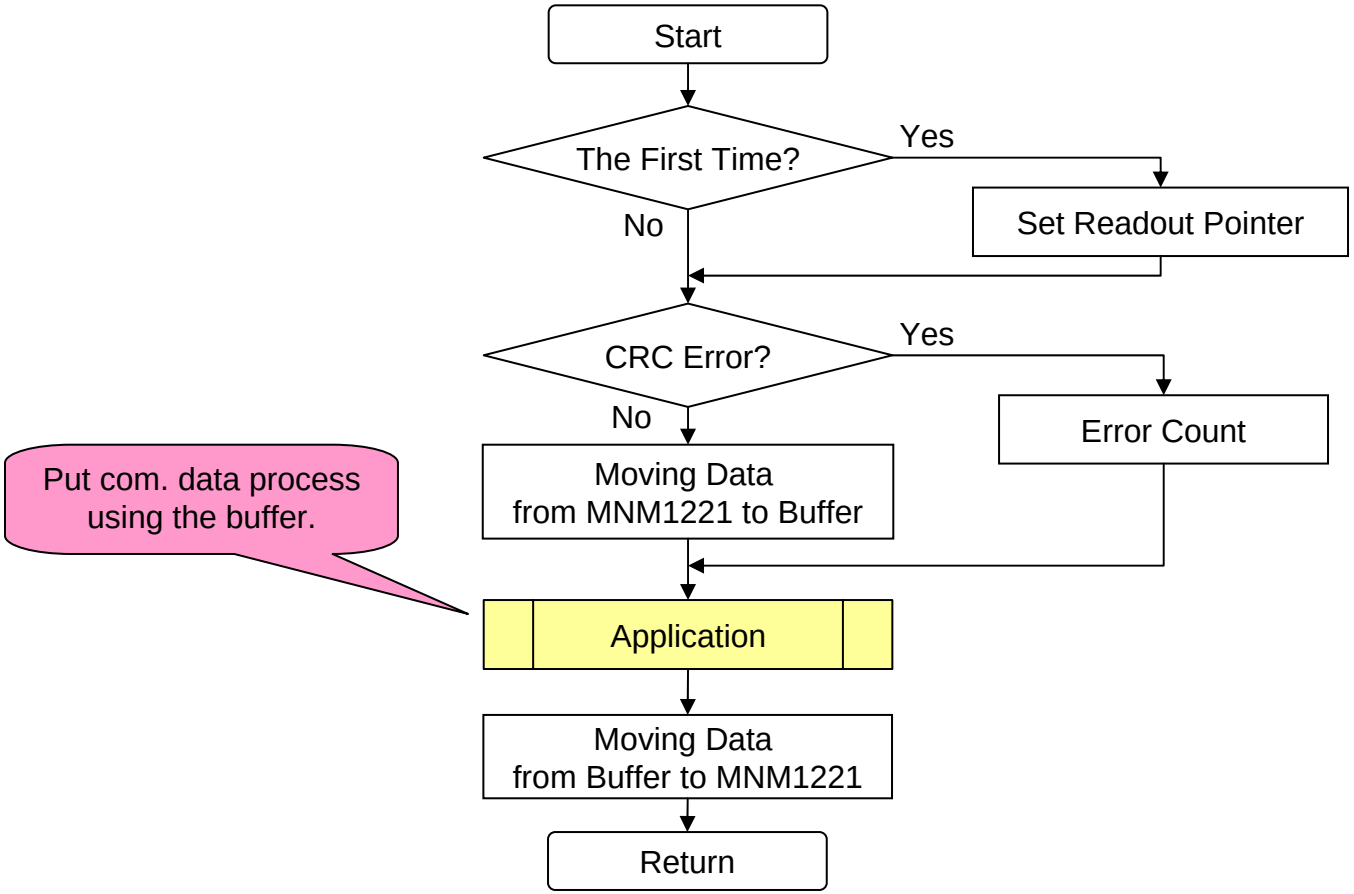
Main Loop

Name	Description
get_state_mnm1221_s()	Reading State



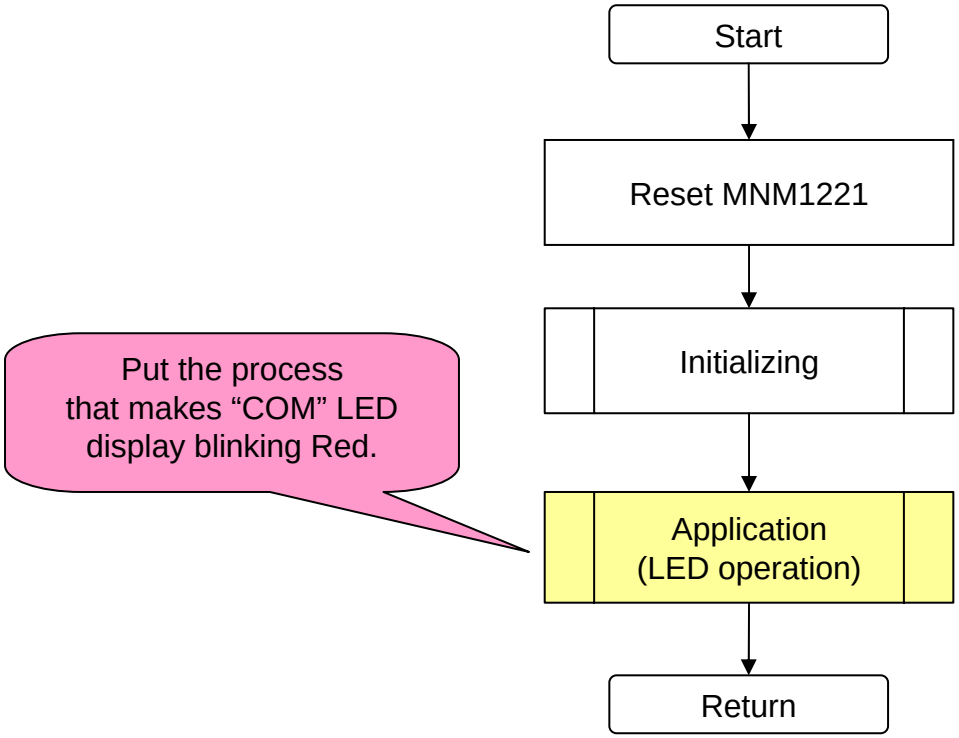
SYNC Interrupt

Name	Description
int_sync_mnm1221_s()	Interrupt by XSYNC of MNM1221



Operation at Timeout Detected

Name	Description
timeout_mnm1221_s()	Initializing at Timeout Detected



TX and RX Buffer Structure

Com. Buffer Structure (16bit)

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The following figure shows my_rx_buf[] when 16bit access. Also my_tx_buf[] .

	Bit 15 – Bit 8	Bit 7 – Bit 0
my_rx_buf[0]	byte1	byte0
my_rx_buf[1]	byte3	byte2
my_rx_buf[2]	byte5	byte4
my_rx_buf[3]	byte7	byte6
my_rx_buf[4]	byte9	byte8
my_rx_buf[5]	byte11	byte10
my_rx_buf[6]	byte13	byte12
my_rx_buf[7]	byte15	byte14

“byte0 to 15” means the contents of the one data block consisting of 16bytes.

Com. Buffer Structure (8bit)

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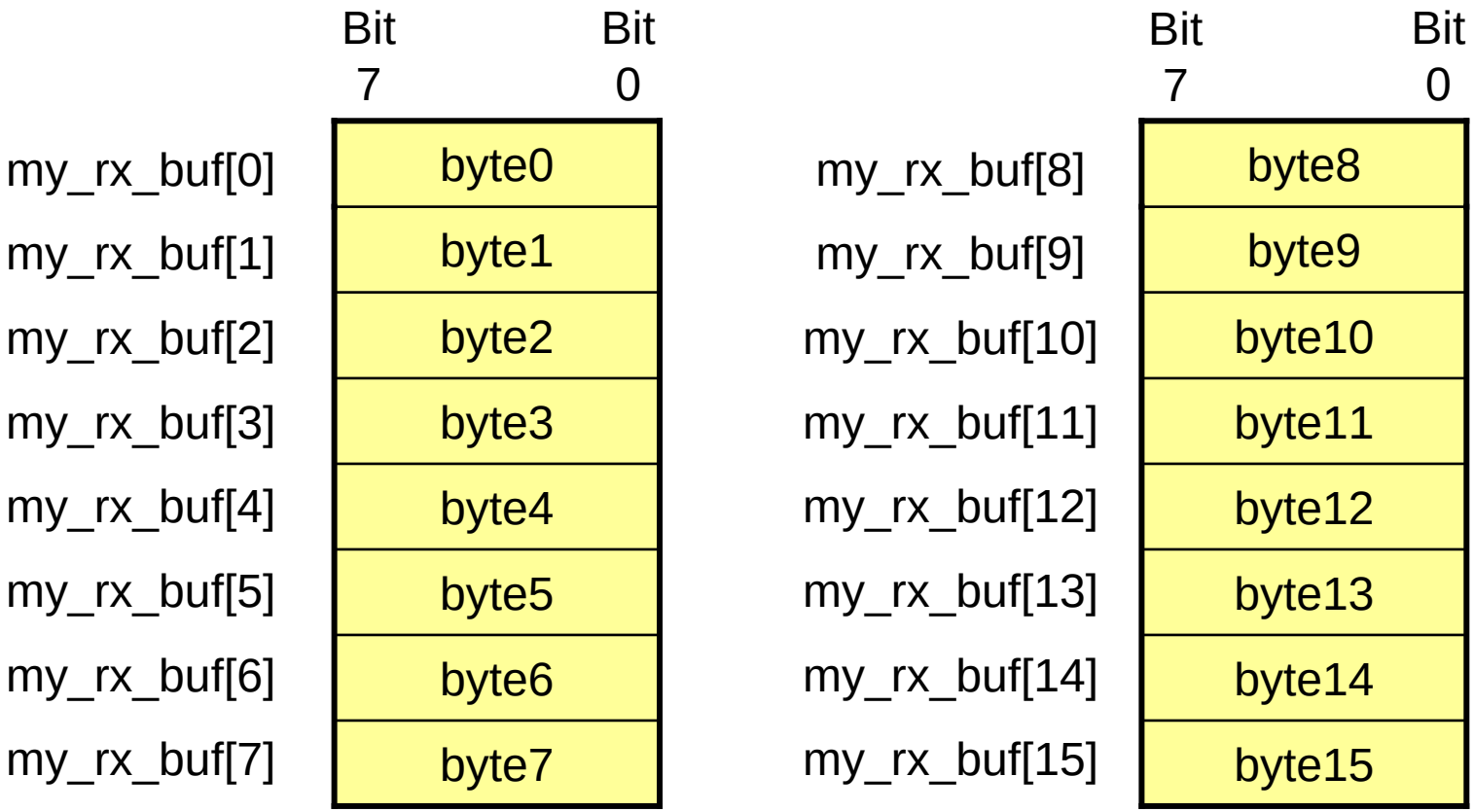
The following figure shows my_rx_buf[] when 8bit access. Also my_tx_buf[] .



“byte0 to 15” means the contents of the one data block consisting of 16bytes.

LED Operation

“COM” LED Operation

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Control the “COM” LED as follows:

Normally

Return Value of get_state_mnm1221_s()	“COM” LED
0x0008 (INITIAL)	OFF
0x0004 (CONFIG-A)	Blinking Green (0.5s ON, 0.5s OFF)
0x0002 (CONFIG-B)	
0x0001 (RUNNING)	Solid Green

Error

Cause of Error	“COM” LED
Timeout	Blinking Red (0.5s ON, 0.5s OFF)
Continuous CRC Error	
Cyclic-data Not Receivable (e.g. MAC-ID Unmatched)	
Out of MAC-ID setting range	Solid Red

Notes:
- Latch an error, and hold the error state until clearing operation even if the cause disappears.
- The Solid Red shows that system reset is needed for clearing.
- The detection time of “Timeout” and “Continuous CRC Error” is typically four communication cycle, and adjust it with careful consideration for safety and noise immunity etc…

Modifying the Example Code

Bus Access Definition

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mnm1221_s.h

```
/*** IMPORTANT!!! ***/
/* You must modify the following definition according to your system. */
/*-------------------------------------------------------------------------*/
/* Definition depend on your system                                        */
/*-------------------------------------------------------------------------*/
/* Located Address of MNM1221 */
#define ADDR_MNM1221        0x08000000      /* unit: byte address */

/* Data Bus Width to access to MNM1221 */
#define SLAVE_16BIT_ACCESS
/* If NOT 16bits BUT 8bits, change this definition to comments or delete it. */
/*-------------------------------------------------------------------------*/
```

Set the address value according to your system.

If 8bit data bus, delete this line.

Occupied Blocks

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mnm1221_s.c

If not one block, change the number of occupied blocks.
(1 block = 16 bytes)

```
/*-----------------------------------------------------------------------*/
/* Definition of constants                                               */
/*-----------------------------------------------------------------------*/

#define N_MY_BLOCK      1       /* the number of my data blocks */
                                /* setting range: 1 to 32, normally 1 */
#if N_MY_BLOCK >= 32
    #define MSK_DATA_CRCE   0xffffffff
#else
    #define MSK_DATA_CRCE   (((unsigned long)1 << N_MY_BLOCK) - 1)
#endif

#define N_MY_DATA       (SIZE_OF_BLOCK * N_MY_BLOCK)
```

Putting Application

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mnm1221_s.c

Int_sync_mnm1221_s()

```
if (!done_1st_cycle) {
    done_1st_cycle = 1;

    order = MNM1221_S_BLK_ORDER & 0x001f;
    p_my_rx_bgn = P_MNM1221_RX_MEM_BGN + (SIZE_OF_BLOCK * order);
    my_dcrc_mask = MSK_DATA_CRCE << order;
}

/* CRC error checking */
crc_err = chk_crc_err(my_dcrc_mask);

/* get command from MNM1221 to my_rx_buf[] */
if (!crc_err) {
    get_cmd_mnm1221();
}

/*--- Here, put your application using my_rx_buf[] and my_tx_buf[] -----*/

/* This function is just for example */
set_resp_example(my_mac_id, crc_err);

/*---------------------------------------- end of your application ---*/

/* set response from my_tx_buf[] to MNM1221 */
set_rsp_mnm1221();
MNM1221_S_TXMEM_SW = 1;                    /* switching TX bank */

return crc_err;
```

Replace this test function with your application.
The time of the calculation must be shorter than communication period.

LED Operation at Timeout

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mnm1221_s.c

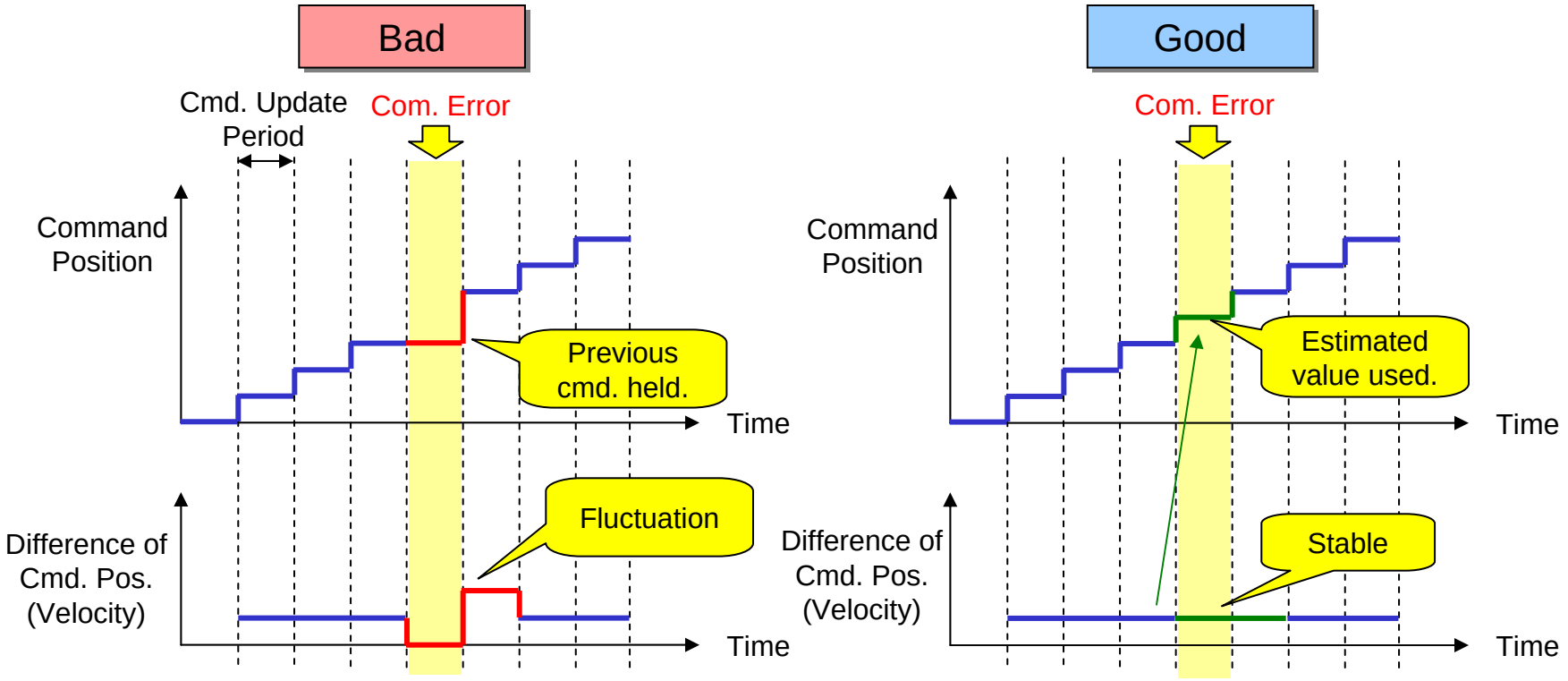
Add the operation of “COM” LED controlling.

```
void timeout_mnm1221_s(short mac_id)
{
    MNM1221_S_RESET = 1;          /* reset MNM1221 */
                                  /* Another way is to control an output port */
                                  /* connected with XRST input of MNM1221. */
    init_mnm1221_s(mac_id);
    /*-------------------------------------------------------------------------*/
    /* Here, put the operation to blink the "COM" LED (ON:0.5s, OFF:0.5s) with red. */
    /*-------------------------------------------------------------------------*/
}
```

Attention for Cyclic Position I/F

Motion at Communication Error

In cyclic position interface device, if the command is held the previous value, that is the same as zero velocity command and causes unstable motion. Therefore, at communication error, the estimated command position on the assumption of constant velocity must be used.



Note: The above description is for momentary communication error. If the error continues over the specific value, the motion must be stopped for safety.

Detection of Data Update Timing

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When data update period is longer than communication period
(e.g. update: 1ms and com.: 0.5ms), recognize the update timing
with the case “continuously twice OK received and update counter changed”.

Previous Receiving	Current Receiving	Update Counter Change	Update Timing?
OK	OK	Change	Yes
OK	OK	Not change	No
Either or Both Error		-	Unknown

Notes:
- “OK” means nothing of both CRC error and frame missing.
- Update Counter is placed at byte0 bit5, 6 in command data block.