



For the traces in this portion, use internal layers and cover with Frame Ground planes.

Connect to an input port of CPU.

Place capacitors close to the following pairs.
pin3-4, 15-16, 28-29, 39-40, 53-54, 78-79, 89-90

At least the following pins require a pull-up resistor individually.

- D00-31
- /XCS
- /TXTIM

Tie the connector shells to Frame Ground.

Void +3.3V and Ground planes underneath the transformer.

Tie to Frame Ground.

"Frame" is the same as "Chassis" Ground.

- The PHY strap pins on this schematic configure as follows:
- Auto-Negotiation Disable
 - 100 Mbps
 - Full-Duplex
 - Auto-MDIX Disable
 - PHY Address: 01h
 - MII Mode

Due to the tight tolerance of voltage ratio setting to "MODE 2" on pin #1 (RX_D3) with R24 and R25, an additional setting on the corresponding MII register is highly recommended as follows:

- Basic Mode Control Register (Addr: 0x0000) = 0x2100;
- 100 Mbps
 - Auto-Negotiation Disable
 - Full-Duplex

When the port of CPU is Hi-Z, this pull-down makes /RESET low.

Connect the /RESET to an output port of CPU. If a watchdog-timer overflows, this /RESET must be set to LOW for safety. Thus, in case of software runaway, all slaves detect timeout and stop with the alarm.

R24 and R25 must be 1% accuracy

U_: with pull-up 50k

D_: with pull-down 50k

T_: 5V Tolerant

Note that RESET_N (pin #18) has an internal pull-up 9k Ohm.

According to required EMC condition, adjust the CR filter close to RESET inputs for both PHY and MNM1221.

Setting for Master 32bits-bus

	MODE1	MODE0	BUSMODE
Master 16bits	0	0	0
Master 32bits	0	0	1
slave 16bits	0	1	0
slave 32bits	0	1	1