MNM1221

100 Mbps Communication ASIC

For RTEX

Datasheet

Motion Control Business Unit

Industrial Device Business Division

Panasonic Industry Co., Ltd.

Revision History

Revision	Date	Change Description	
0.1	2004/5/6	Initial Release (Preliminary)	
1	2011/9/13	P1	Changed title and company name.
		P8	Updated introduction and features.
		P10	Updated recommended PHY.
		P15	Clarified timing between XSYNC and transmitting.
		P16	Clarified that JTAG pins cannot be used in normal operation.
		P25	Updated communication period description.
		P27	Clarified description for RX bank switching.
		P39	Corrected period setting value.
		P46	Renamed “recovering function” to “error correcting function”.
		P51-56	Added MII register access section.
		P57-94	Added slave operation chapter. Renamed “Servo slave” to “Generic slave”.
		P97	Added maximum current consumption.
		P102	Added ordering information.
2	2012/2/22	P16	Added pin16 as ADDVDD and pin61 as ADDVSS.
3	2024/5/9	P10	Updated the recommended PHY and magnetics.
		P16	Added 5T as XRST type.
		P24-25	Added “Frame Structure”.
		P26-29	Added “Frame Descriptions”.
		P30	Modified “Time Chart at Start-up”.
		P31	Updated the communication period.
		P38	Added the descriptions on “Chip Reset”.
		P45	Updated the setting example on “Transmission Period”.
		P48	Modified Frame ID description on “Communication State”.
		P50-53	Clarified the descriptions on “Error Flags 1, 2”.
		P69-71	Corrected the condition of the state change for RUNNING.
		P78	Added the descriptions on “Chip Reset”.
		P88	Modified Frame ID description on “Communication State”.
		P90-91	Clarified the descriptions on “Error Flags”.
		P108-109	Added the description for XWAIT.

Table of Contents

Chapter 1
General Description

Overview

Introduction

MNM1221 is a serial interface controller ASIC that enables to establish the real-time communication systems "*Realtime Express (RTEX)*" based upon the master-slaves communication style with the ring topology. The MNM1221 requires to be used with a PHY (PHYsical layer chip), a pulse transformer and shielded twisted pair cables for 100BASE-TX (IEEE 802.3u) system. In other words, MNM1221 is a special MAC(Media Access Controller) in order to suit 100BASE-TX to real-time communication system for the multi-axis servo control.

The MNM1221 serial interface system consists of one master and several slaves, and exchanges the command data from the master and the response data from the slave cyclically. For that, MNM1221 has double banks (buffer) memory for each transmitting and receiving, and this function allows the CPU to operate efficiently.

Features

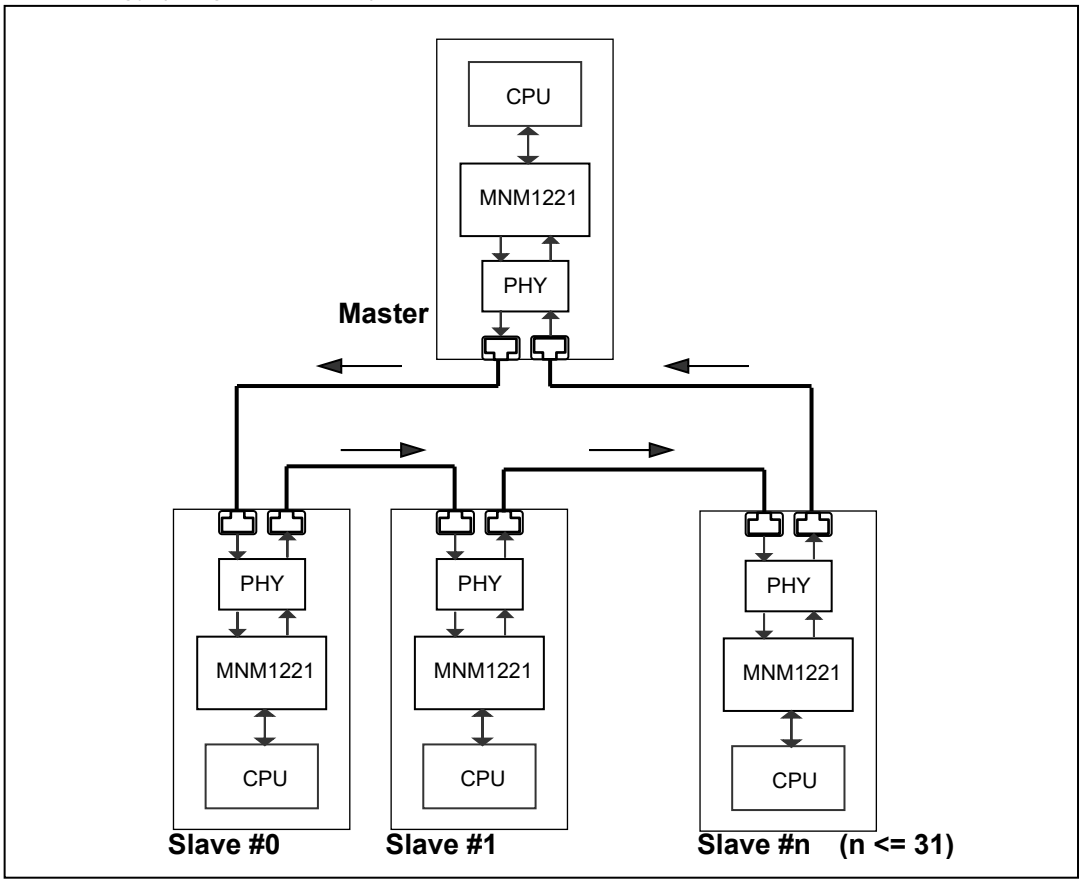
- Connected to the PHY with MII (Media Independent Interface) by IEEE 802.3u
- Ring topology
- 100 Mbps Full-Duplex
- For both master and slave mode operation
- Maximum 32 slaves
- Double banks (buffer) memory, size of 512 bytes each for RX and TX.
- Data bus for CPU interface:
  Master: 32-bit or 16-bit wide
  Slave: 16-bit or 8-bit wide
- Data error detection based on CRC-CCITT(16bits CRC)
- 25MHz clock same as driving PHY
- 3.3V operation and partly with 5 V tolerant pins for CPU interface
- -40 to +85 deg C operating ambient
- 100 pins plastic LQFP package of Pb-Free

Applications

- High performance multi-axis servo control systems

System Diagram

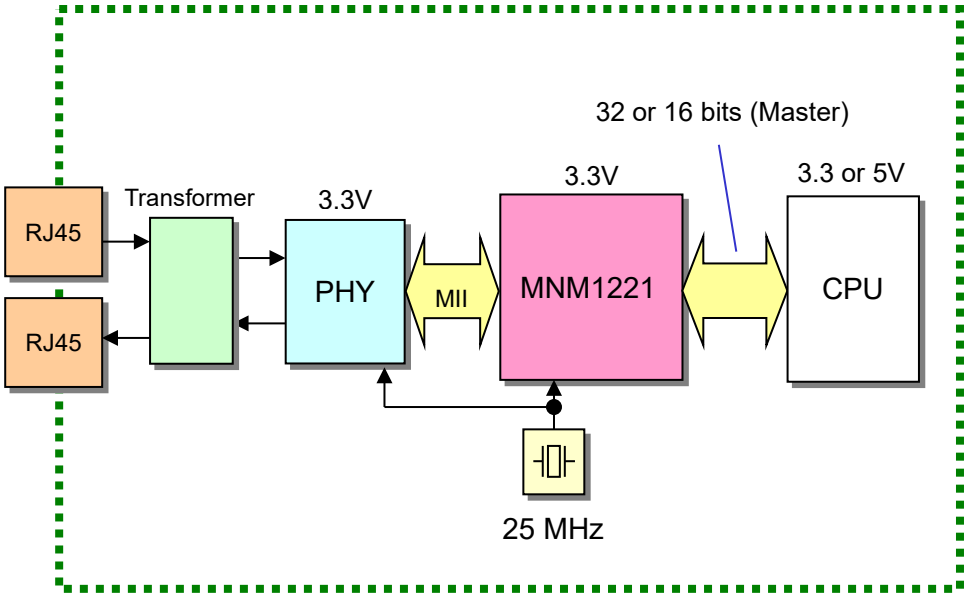
Topology (Ring connection)



Notes:

- A hub, required in normal 100BASE-TX system, is not used because of Ring topology.
- Pulse transformers are omitted in the figure.
- STP(Shielded Twisted Pair cable) conforming to CAT5e(category 5 enhanced) or upper should be used.

Detail of a Node



Notes about PHY chip:

The pin configuration for the operation must be set as follows. Some PHYs such as DP83822 by TI need MII register setting as well.

- Fixed Full-Duplex
- Disable Auto-Negotiation
- Force 100BASE-TX mode
- Disable Auto-MDIX

Recommended PHY:

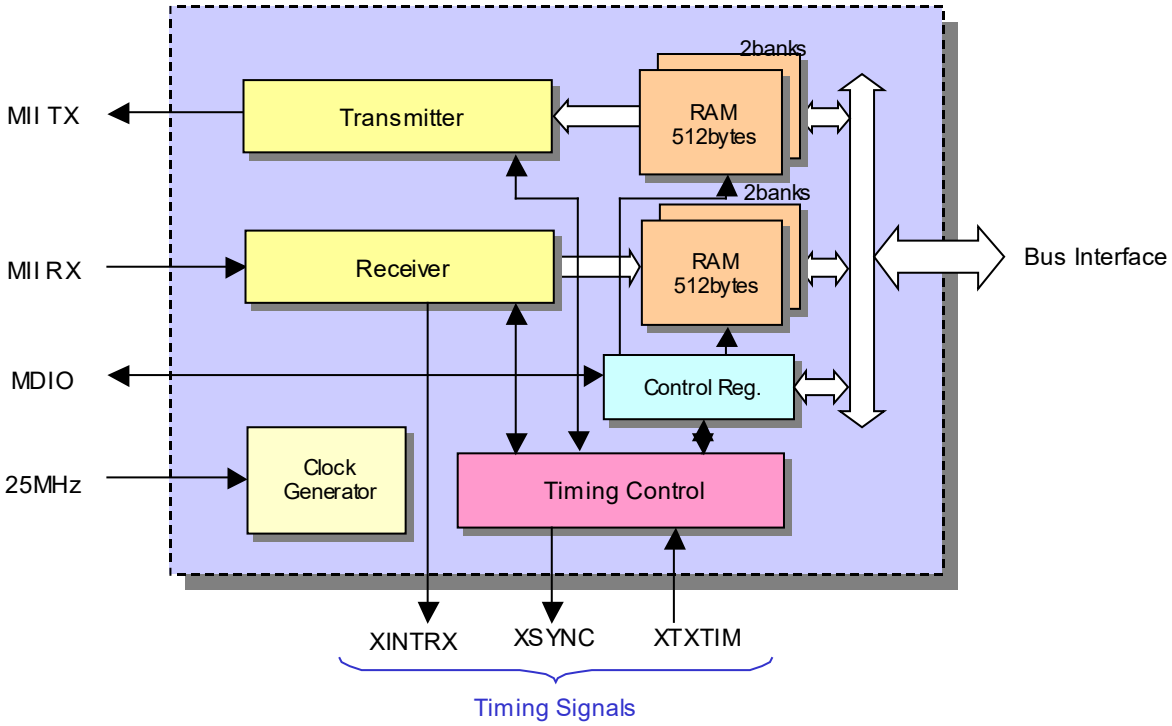
Manufacturer	Part Number	Package	Ambient Temp.
Broadcom	BCM5221KPTG	QFP 64 pins	-40 to +85 deg C
TI	DP83848IVV	QFP 48 pins	-40 to +85 deg C
TI	DP83822IRHBR	QFN 32 pins	-40 to +85 deg C

The pulse transformer (magnetics) suited to each PHY must be selected.

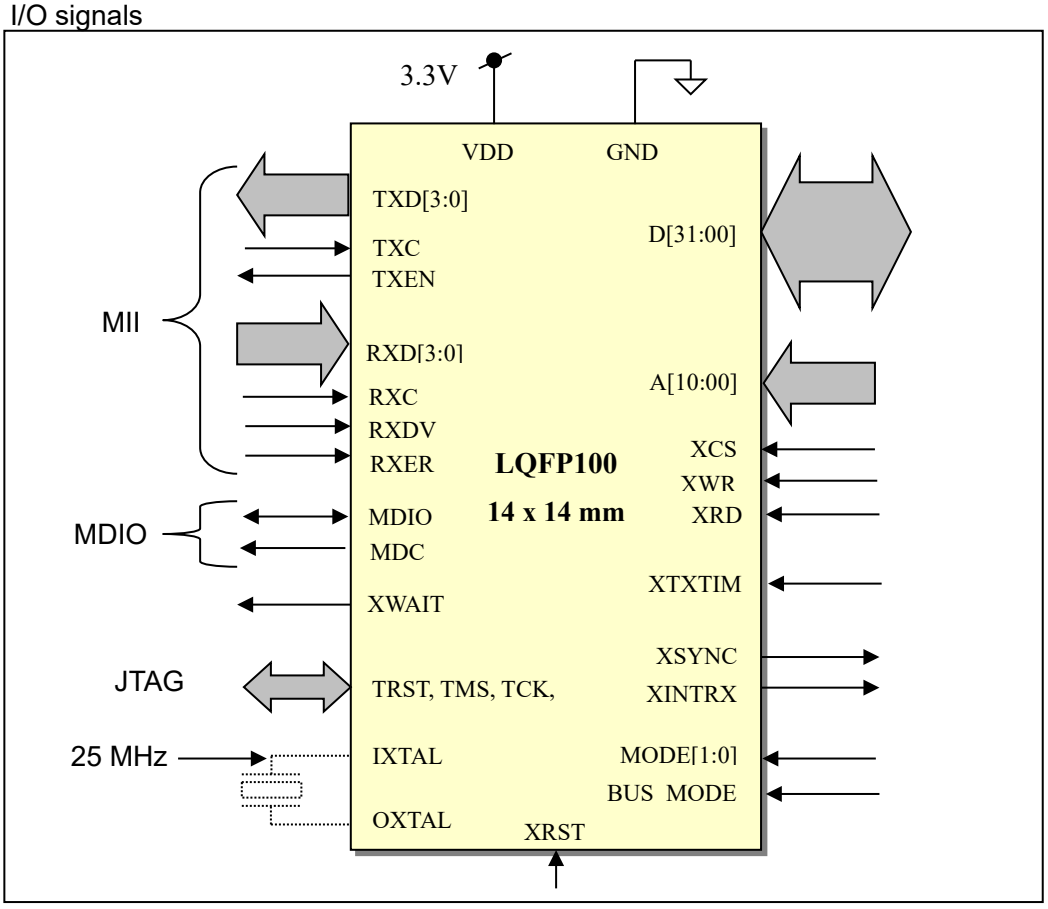
The following is an example. RJ45 connector with built-in magnetics cannot be used.

Manufacturer	Part Number	Ambient Temp.
Bothhand	TS8121CM HF	-40 to +85 deg C
Bothhand	TS21C HF	0 to +70 deg C

Block Diagram of MNM1221

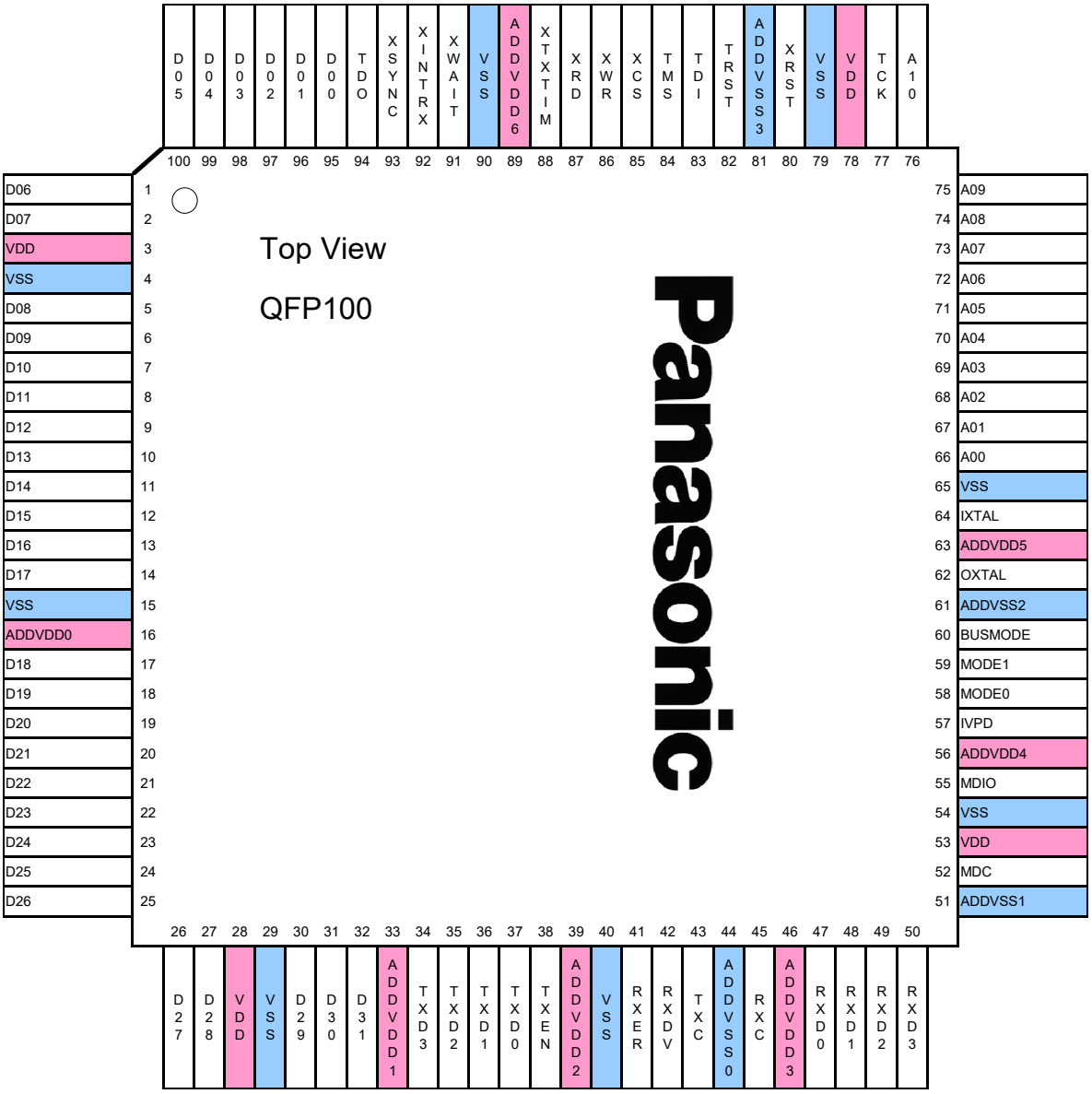


I/O signals



Pin Descriptions

Pin Assignments



Note:

Ceramic capacitors of about 0.1 uF should be put close to each pair of VDD and VSS.

Master Pin Descriptions

Name:

Prefix	Description
“X”	Negative Logic
Non	Positive or Non Logic

Type:

Symbol	Description
I	Input
O	Output
I/O	Input/Output
I_{PD}	Input with internal Pull-Down register
I_{PU}	Input with internal Pull-UP register
5T	5 V Tolerant

Mode:

<table>
<tr><th>Name</th><th>Pin#</th><th>Type</th><th>Description</th></tr>
<tr><td>MODE1,
MODE0</td><td>59
58</td><td>I_{PD}
I_{PD}
5T</td><td>Mode Selection:
The operating mode is defined by MODE[1:0].
Connect both MODE1 and 0 to GND directly.

<table>
<tr><th>MODE 1</th><th>MODE 0</th><th>Operating mode selected</th></tr>
<tr><td>Low</td><td>Low</td><td>Master</td></tr>
<tr><td>Low</td><td>High</td><td rowspan="3">Do not set</td></tr>
<tr><td>High</td><td>Low</td></tr>
<tr><td>High</td><td>High</td></tr>
</table>
</td></tr>
<tr><td>BUSMODE</td><td>60</td><td>I_{PD}
5T</td><td>Bus Mode Selection:
The bus size for CPU interface is defined by BUSMODE.
Connect to either GND or VDD(3.3 V) directly.

In Master mode:
<table>
<tr><th>BUSMODE</th><th>Data</th><th>Address</th></tr>
<tr><td>Low</td><td>D[15:0]</td><td>A[10:1]</td></tr>
<tr><td>High</td><td>D[31:0]</td><td>A[10:2]</td></tr>
</table>
</td></tr>
</table>

MII:

Name	Pin#	Type	Description	At Reset
TXC	43	I	**MII Transmit Clock:** TXC is the transmit clock from PHY. The frequency is 25 MHz. A dumping register that is about 33 Ohm should be put near the output pin of the PHY.	
TXD[3:0]	34-37	O	**MII Transmit Data Output:** TXD[3:0] are the transmit data synchronized with TXC.	L
TXEN	38	O	**MII Transmit Enable:** Indicates that the data on TXD[3:0] is valid.	L
RXC	45	I	**MII Receive Clock:** RXC is the receiving clock from PHY. The frequency is 25 MHz A dumping register that is about 33ohm should be put near the output pin of the PHY.	
RXD[3:0]	47-50	I	**MII Receive Data Input:** RXD[3:0] are the receiving data synchronized with RXC.	
RXDV	42	I	**MII Receive Data Valid:** Indicates that the data presented on RXD3-0 is valid.	
RXER	41	I	**MII Receive Error Detected:** Indicates that an error is occurring during a receiving frame.	
MDIO	55	I/O	**Management Data I/O:** This serial input/output is used to read from and write to the MII registers in the PHY. MDIO is synchronized with MDC. An external pull-up register that is about 1.5 k Ohm must be put.	HiZ
MDC	52	O	**Management Data Clock:** MDC is the clock output for serial interface of MDIO. The frequency is 781.25 kHz.	L

CPU interface:

Name	Pin#	Type	Description	At Reset
D[31:0]	1,2, 5-14, 17-27, 30-32, 95-100	I/O 5T	**Data Bus:** Either 16bits-width via D[15:0] or 32 bits-width via D[31:0] can be used. The 32 bits-width is more recommended for the faster access. In 16 bits case, unused D[31:16] should be pull-downed with external registers that are about 10 k Ohm.	HiZ
A[10:0]	66-76	I 5T	**Address Bus:** The address data is 11bits-wide via A10-0. But A0 is not used in 16bits data bus, additionally A1 is not used in 32 bits data bus. Therefore, the followings are recommended: 16 bit bus: Connect A0 to GND. 32 bit bus: Connect both A0 and A1 to GND.	
XCS	85	I 5T	**Chip Select:** For this chip selection. Low active.	
XRD	87	I 5T	**Read (Output) Enable:** For read access. Low active.	
XWR	86	I 5T	**Write Enable:** For write access. Low active.	
XWAIT	91	O	**Wait Request:** XWAIT indicates the waiting requirement during an access. To ensure the access, XWAIT should be connected to the wait input pin of the CPU. Low active.	H

Timing signals:

Name	Pin#	Type	Description	At Reset
XSYNC	93	O	**Transmitted Timing Pulse:** XSYNC is outputted when starting transmitting the frame. At this pulse output, the transmitting has already started. The falling edge is effective. The pulse width is 1.28 us.	H
XINTRX	92	O	**Receiving Interrupt Pulse:** XINTRX is outputted when completing receiving the frame. The falling edge is effective. The pulse width is 1.28 us.	H
XTXTIM	88	I 5T	**Transmit Timing:** When using an external timing signal to start transmitting the frame in the running state, the cyclical trigger signal is required to input into XTXTIM. In this case, the register setting must be needed to switch from the internal timing signal that is default. XTXTIM is ignored out of the running state. The falling edge is effective. When not using XTXTIM, connect to VDD(3.3 V).	

Clock and Reset:

Name	Pin#	Type	Description
OXTAL IXTAL	62 64	I/O I	**Crystal Output and Input for MII:** IXTAL must be driven with a 25 MHz oscillator clock that is the same as driving PHY chip. Accuracy is +/- 50 ppm. OXTAL must be left unconnected. A dumping register that is about 33 Ohm should be put near the output pin of the oscillator.
XRST	80	I 5T	**Reset input:** Hardware reset input. Low active.

JTAG(Boundary Scan):

These pins are for factory test only. For normal operation, these pins cannot be used.

Name	Pin#	Type	Description
TCK	77	I_{PU}	**JTAG Clock:** JTAG clock input. This pin should be connected to VDD(3.3 V).
TRST	82	I_{PU}	**JTAG Reset:** JTAG reset input. Low active. This pin should be connected to GND.
TMS	84	I_{PU}	**JTAG Mode Select:** JTAG mode select input. This pin should be connected to VDD(3.3 V).
TDI	83	I_{PU}	**JTAG Data Input:** JTAG data input. This pin should be connected to VDD(3.3 V).
TDO	94	O	**JTAG Data Output:** JTAG data output. This pin must be left unconnected.

Power:

Name	Pin#	Type	Description
VDD	3,28, 53,78		V_{DD}=3.3 V Put decoupling ceramic-capacitors between VDD and VSS pairs close to MNM1221.
VSS	4,15,29, 40,54, 65,79 90		V_{SS}=GND
ADDVDD	16,33, 39,46, 56,63, 89		V_{DD}=3.3 V Put decoupling ceramic-capacitors between VDD and VSS pairs close to MNM1221.
ADDVSS	44,51, 61,81		V_{SS}=GND
IVPD	57	I	IVPD must be connected directly to GND. This is for an internal protection of the chip.

Slave Pin Descriptions

The pins having the different functions from in master are described as follows:

Mode:

Name	Pin#	Type	Description
MODE1, MODE0	59 58	I_{PD} I_{PD} 5T	**Mode Selection:** The operating mode is set. See “Operating Mode Settings”.
BUSMODE	60	I_{PD} 5T	**Bus Mode Selection:** Data bus width (servo) or MAC-ID type (IN/OUT) is set. See “Operating Mode Settings”.

CPU interface:

Name	Pin#	Type	Description	At Reset
XWAIT / XLED	91	O	**Wait Request (Generic slave):** To ensure the access, XWAIT should be connected to the wait input pin of the CPU. Low active. **LED output (IN or OUT slave):** In RUNNING state and not timeout, Low is outputted. This signal is used for driving status LED. In addition, the detection time of timeout is 20.9 ms.	H

Timing signals:

Name	Pin#	Type	Description	At Reset
XSYNC	93	O	**Synchronizing Timing Pulse:** After all slaves receive the frame in RUNNING state, this pin outputs negative pulse at the same time in all slaves. In only RUNNING state, this signal is outputted. The falling edge is effective. The pulse width is 1.28 us.	H
XINTRX	92	O	**Receiving Interrupt Pulse:** XINTRX is outputted at receiving the frame completely. The falling edge is effective. The pulse width is 1.28 us.	H
XTXTIM	88	I 5T	**Transmit Timing:** Connect to VDD because of no function in slave mode.	

Operating Mode Settings

MNM1221 reads MODE[1:0] and BUSMODE pins after reset, and sets the operating mode as following table. These pins must be connected to VDD or GND directly according to each operating mode. In addition, these pins are read only once after reset.

MODE1	MODE0	BUSMODE	Operating Mode	Data pins	Address pins	Pin 91
L	L	L	Master	D[15:0]	A[10:1]	XWAIT
		H		D[31:0]	A[10:2]	
	H	L	Generic Slave	D[15:0]	A[10:1]	
		H		D[7:0]	A[10:0]	
H	L	L	IN Slave	D[31:0] (IN fixed)	A[4:0] (BIN)	XLED
		H			A[5:0] (BCD)	
	H	L	OUT Slave	D[31:0] (OUT fixed)	A[4:0] (BIN)	
		H			A[5:0] (BCD)	

Notes:

- Unused pins should be connected as follows:
  Data ……. Pulled down with 10 k Ohm. However, if OUT slave, it may be open.
  Address … Connect to GND directly.

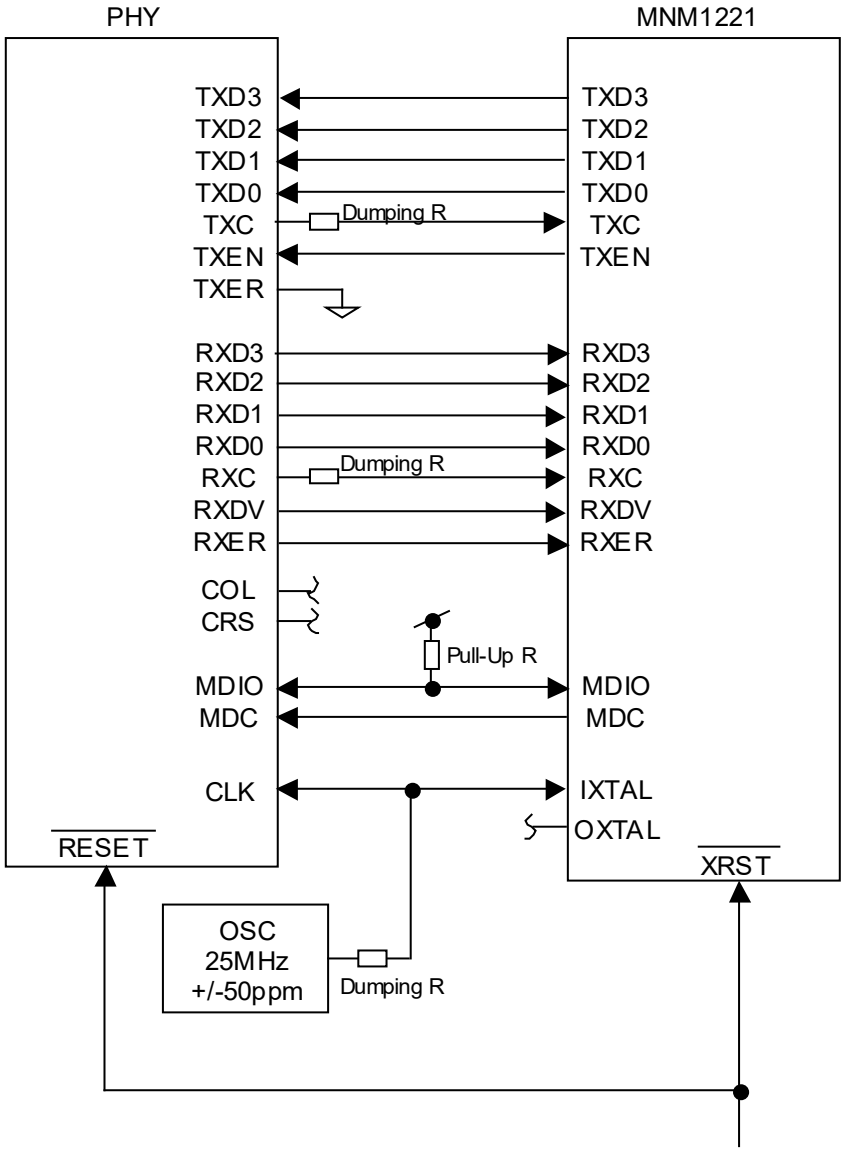
- In IN/OUT slave, the data bus behaves to input or output pins for external interface.

- In IN/OUT slave, the address bus behaves to MAC-ID inputs which are read only once after reset. Also, either BIN or BCD as data type is selected with BUSMODE pin.

- In IN/OUT slave, Pin91 performs as XLED pin.

- In OUT slave, Low is outputted until receiving the first valid data after reset. Therefore, the system that is in safety side when Low is outputted must be designed. Also, since the data bus becomes Hi-Z during reset, pull-down resistors of about 10 k Ohm must be added to make stable level.

Connection to PHY with MII



Notes:

- Approximately 33 Ohm is suitable for the dumping registers to reduce reflections.
- The value of the pull-up register on MDIO depends on PHY. It is approximately 1.5 k Ohm.
- The line length should be traced as short as possible.

Chapter 2
Master Operation

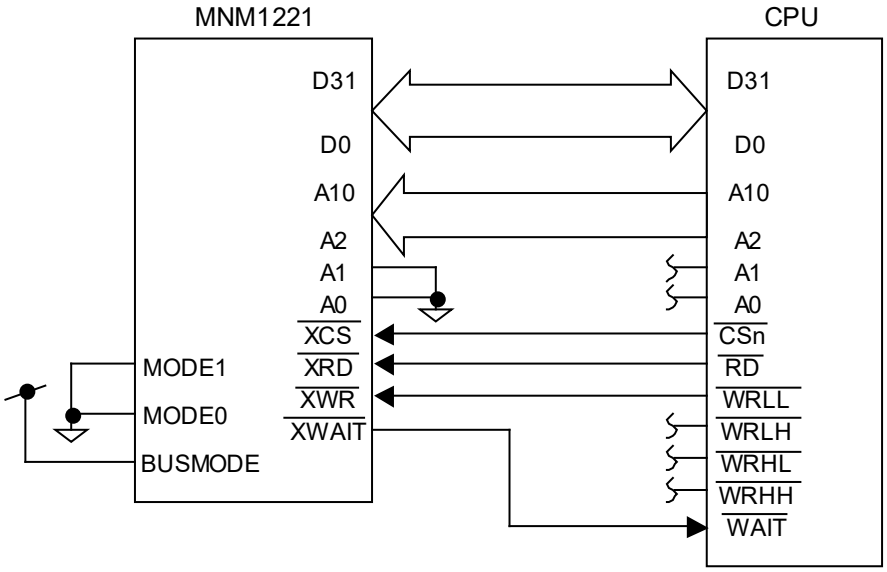
Connection for Master Operation

Mode Setting

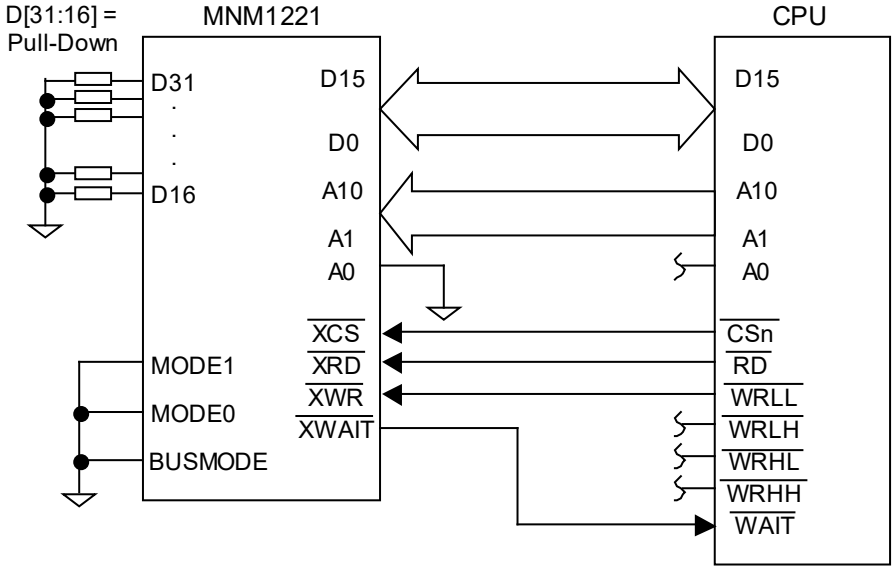
MNM1221 has two operating modes that are Master and Slave, and this document describes only Master mode. In Master mode, both MODE1 and MODE0 pins must be connected to GND.

Bus interface between MNM1221 and CPU

32 bits bus (BUSMODE = High):



16 bits bus (BUSMODE = Low):



Note: Approximately 10 k Ohm is suitable for the pull-down registers on D[31:16].

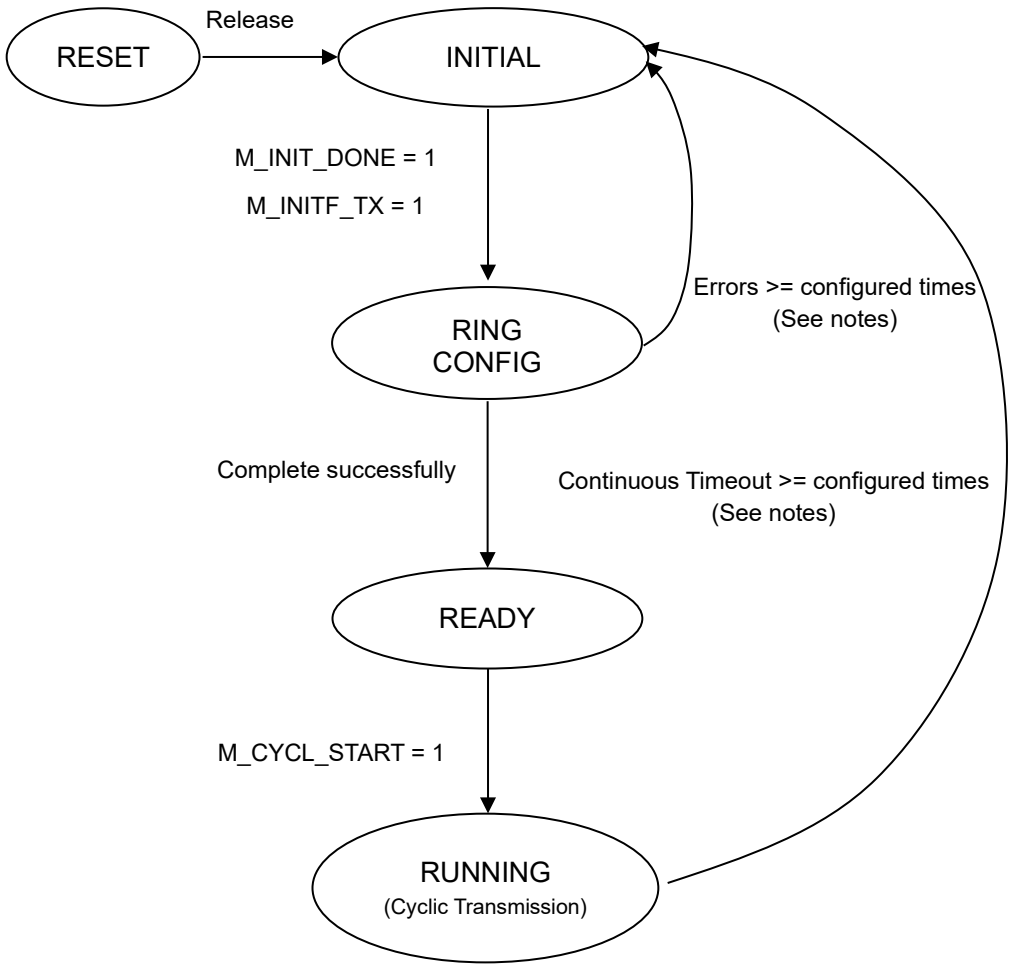
The above figure shows an example of CPU with byte-unit address bus.

Functional Description

State Transition of MNM1221

Before reaching RUNNING state that performs cyclic transmission, it goes through the process showed the following figure.

"M_…": control registers



Notes:

- In RING CONFIG or RUNNING, M_ERR_COUNT configures the conditions changing to INITIAL.
- If M_RESET is set to 1 in any state, the state becomes INITIAL.

Descriptions of Each State

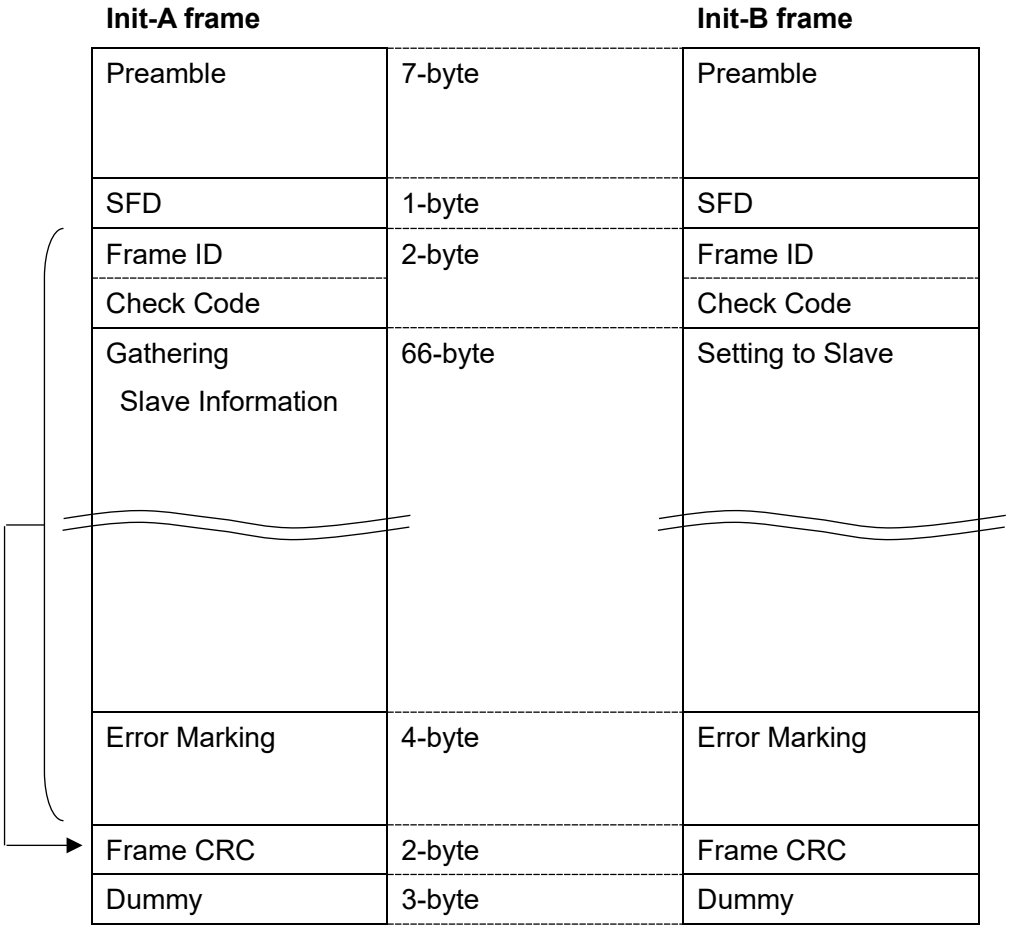
State	Descriptions	Communication	
		Frame Name	Period
INITIAL	The firmware is initializing the registers in MNM1221. e.g.) Transmitting period in RUNNING state	-	-
RING CONFIG	MNM1221 is searching for the information about each Slave, and configuring the operation. As a result of the process, the information is stored into the status registers. e.g.) The sum of Slaves, MAC-IDs etc… For that, two initial frames are automatically transmitted. The firmware is waiting for READY state after finished the process.	Init-A Init-B	2 ms
READY	MNM1221 is ready to proceed to RUNNING state. After checking the Slave information, the firmware instructs MNM1221 to proceed to RUNNING state.	-	-
RUNNING	Using TX and RX memory in MNM1221, the firmware is communicating cyclically.	Real-time	XTXTIM or Internal timer

Notes:

- In RING CONFIG state, using the internal timer, MNM1221 transmits the initial frames by itself. If Slave is not established yet and Initial Error field in M_ERR_COUNT register is set to 0, the initial frame transmission is repeated.

- In READY state, the firmware confirms whether the sampled Slave information is the same as the intended one. If not, it must not proceed to RUNNING state.

Frame Structure

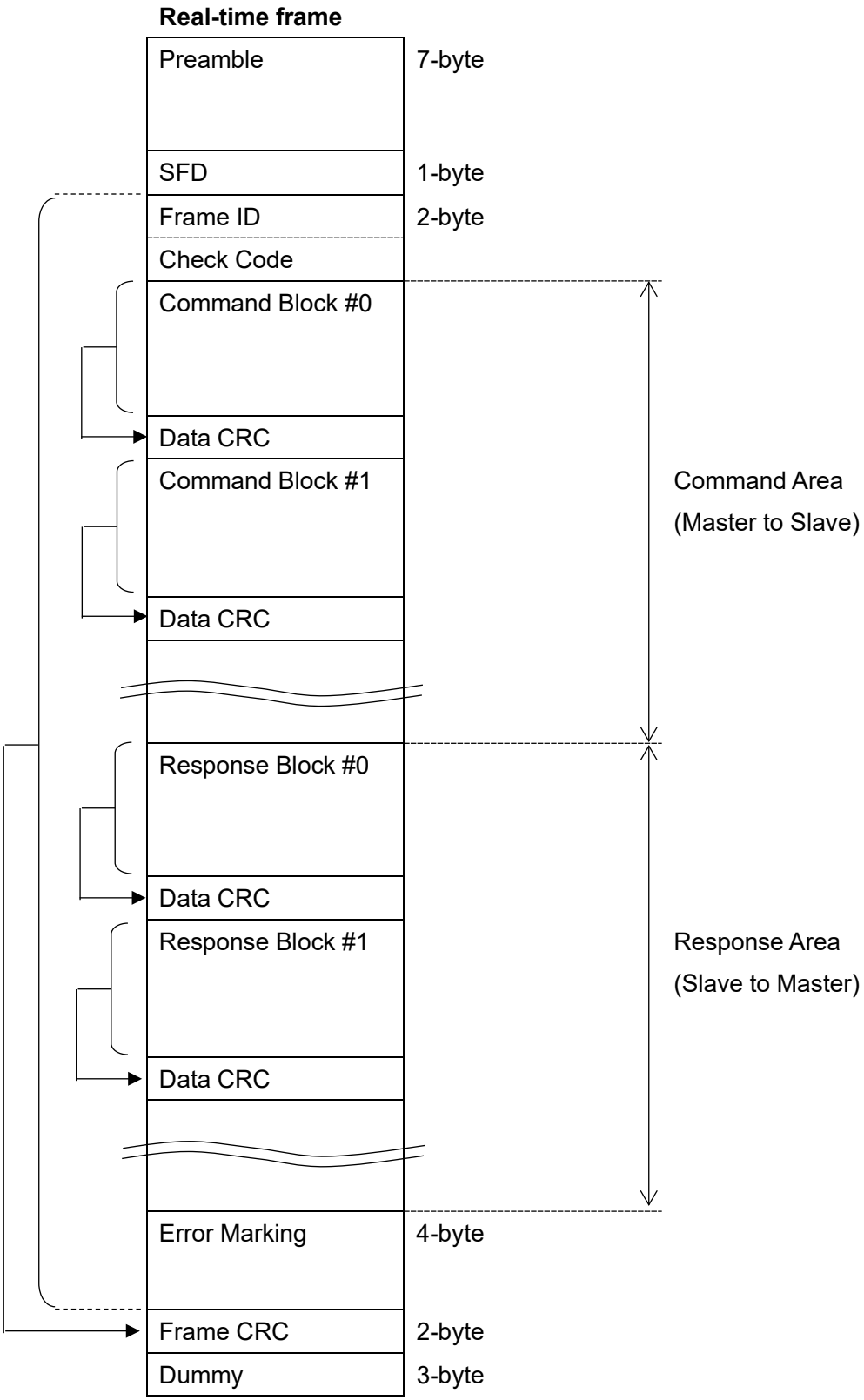


Init-A frame		Init-B frame
Preamble	7-byte	Preamble
SFD	1-byte	SFD
Frame ID	2-byte	Frame ID
Check Code		Check Code
Gathering Slave Information	66-byte	Setting to Slave
Error Marking	4-byte	Error Marking
Frame CRC	2-byte	Frame CRC
Dummy	3-byte	Dummy

Preamble: every 55h

SFD: D5h

Dummy: 00h


Real-time frame
Preamble
7-byte
SFD
1-byte
Frame ID
2-byte
Check Code
Command Block #0
Data CRC
Command Block #1
Data CRC
Command Area
(Master to Slave)
Response Block #0
Data CRC
Response Block #1
Data CRC
Response Area
(Slave to Master)
Error Marking
4-byte
Frame CRC
2-byte
Dummy
3-byte

Frame Descriptions

Frame Types and Flow

There are three types of the frames: Init-A, Init-B and Real-time.
For each frame, the master transmits the frame first. When the first slave receives the frame, it writes data inside it and then transmits it. If multiple slaves are connected, the subsequent slaves will perform the same operation. Finally, the master receives the frame that all slaves have finished writing. The master is always the first to send a frame and the slaves never send frames voluntarily.

Init-A, Init-B Frames

These frames are used in the RING CONFIG state. The master gathers the information about each slave with the Init-A frame, and the master sets control data to each slave with the Init-B frame.

Real-time Frame

This frame is used for data exchange between the master and the slaves in RUNNING state. The block which consists of 16 bytes is the unit of the exchange.
The inside of the frame is divided into areas for commands from the master to the slaves and responses from the slaves to the master. Inside each area, the data blocks occupied by each slave are arranged in the order of cable connection, first the blocks of the first slave, then the blocks of the second slave. The number of blocks each slave occupies is configured to range from 1 to 32, but there is a maximum limit of 32 blocks in an area. The frame length changes depending on the number of blocks in the area.
The command/response area in this frame corresponds to the TX/RX memory in MNM1221.
In the command area, after the master writes data to all blocks and sends it, each slave reads data from the block it occupies. In the response area, after the master sends data with an initial value of 0, each slave writes response data to the block it occupies. After receiving the frame, the master reads data from all blocks.

Preamble, SFD (Start Frame Delimiter)

These are frame start codes specified by IEEE 802.3.
MNM1221 recognizes the beginning with Preamble 1-byte and SFD. Therefore, even if the Preamble is missing 6-byte, it can receive the frame normally. In the slave, the Preamble of the received frame is replaced with a new one before transmitting.

Frame ID

MNM1221 distinguishes the frame type with the Frame ID.
The Frame ID is inverted to the Check Code which is used to detect ID error.

	Init-A	Init-B	Real-time
Frame ID	81h	DBh	7Eh
Check Code	7Eh	24h	81h

Discarding Frame

The received frame is discarded in the following situations:

- An error is detected on the Frame ID.
- An interruption during reception makes the frame length shorter.

In this case, MNM1221 will not output XINTRX, and not output XSYNC on the slave either.
In addition, since the slave does not transmit the frame, it is lost in subsequent nodes.

CRC

There are two CRCs, Frame CRC and Data CRC, based on the difference in the target area for detecting data error. The CRC specifications for both are as follows:

Code	CRC-CCITT
Generator Polynomial	$X^{16} + X^{12} + X^5 + 1$
Initial Value	0
Shift Direction	Left

Frame CRC

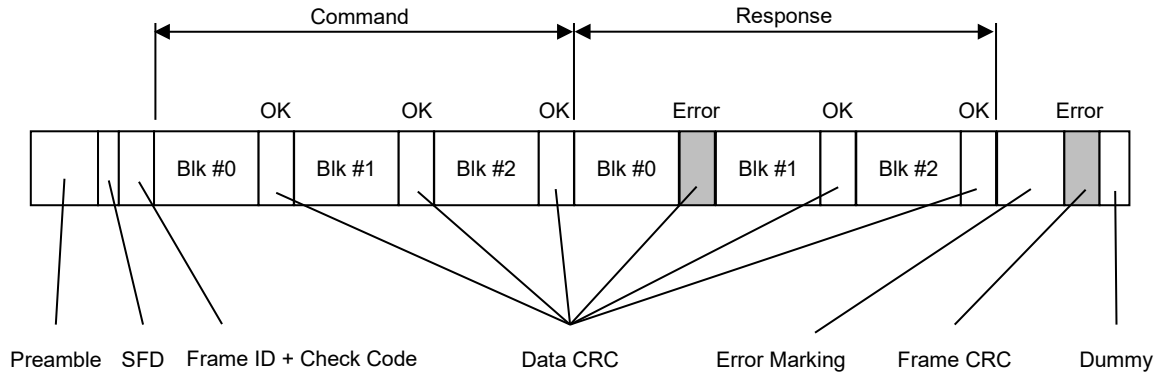
The Frame CRC in every frame checks all data within the frame. Since some data always changes when the frame passes through the slave, it is replaced with a newly calculated Frame CRC at the same time.

Error Marking

If the slave detects a Frame CRC error when receiving a frame, it records the error in the Error Marking and then updates the Frame CRC. This notifies subsequent nodes that an error has been detected.

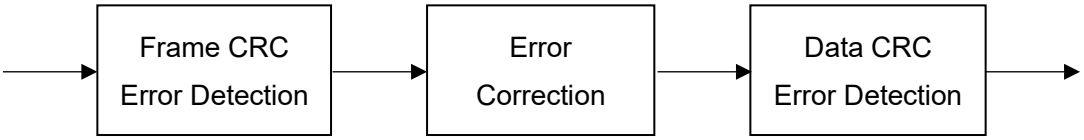
Data CRC

The Data CRC in the Real-time frame checks one block within the command or response area. When the frame passes through the slave, the response block occupied by that slave changes, so only the Data CRC of that part is replaced with the newly calculated one. Since the command block is only read by the slave and does not change, the Data CRC does not change either. The Data CRC is attached to each block, so if there are multiple blocks that partially show an error, the blocks that show OK can be used. For example, in the following figure which shows three blocks frame, the response block #0 cannot be used due to Data CRC error. However, the other blocks can be used since Data CRC shows OK. In addition, when the Data CRC shows error, ether the Frame CRC or the Error Marking shows error.



Error Correction and CRC Error

MNM1221 has the error correction function, so even if the command/response blocks in the Real-time frame are corrupted, they will be automatically restored upon reception. However, there is a limit to the ability of this function, and if restoration is not possible, the Data CRC will show an error. On the other hand, since error detection using the Frame CRC checks the blocks before the error correction, it may happen that "All Data CRCs are OK, but Frame CRC is an error.". The blocks whose Data CRC indicates OK can be used regardless of the Frame CRC, so use only the Data CRC to determine usability.

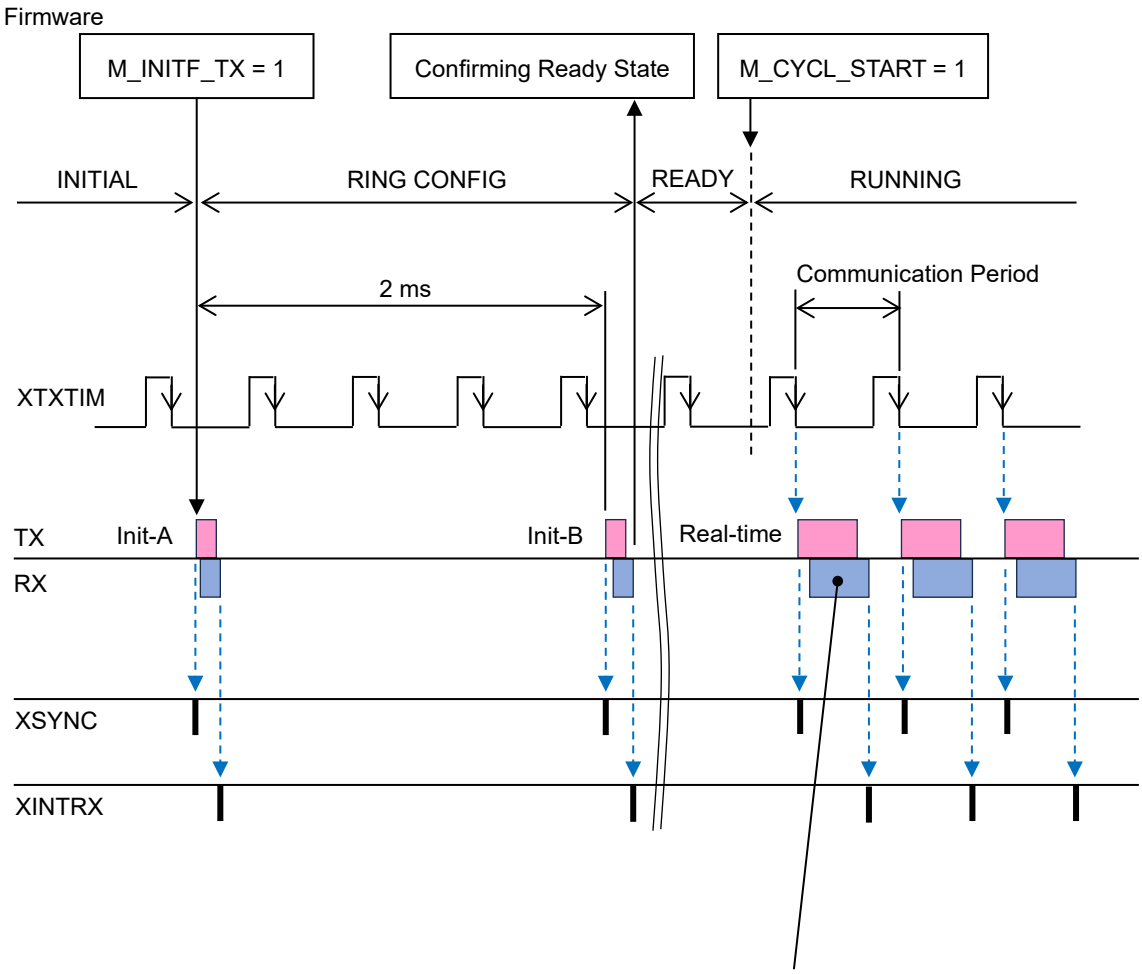


Dummy

The Dummy is used by MNM1221 for timing control.

Time Chart at Start-up

The following chart shows the case using XTXTIM for TX trigger in RUNNING state.



Ignore the contents of the first RX frame because of invalid data.

Transmission in RUNNING State

Communication (Transmitting) Period:

Communication period, that is the same as transmitting period, can't be set up freely because it must be synchronized with servo control. According to servo specifications, the period must be set to suitable value as accurately as possible. In servo A6N, the communication period must be selected from 2 ms, 1 ms, 0.5ms, 0.25 ms, 0.125 ms, and 0.0625 ms. The command update period is the same or twice as the communication period. The default setting of the servo is that the communication period is 0.5 ms and the command update period is 1 ms.

Default setting of the servo:

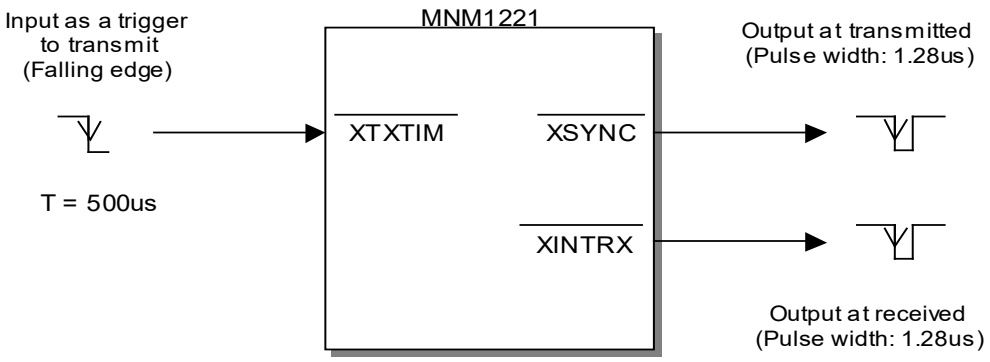
Communication period (Frame transmitting period)	0.5 ms
Command update period (Command is on the frame.)	1 ms

Timing Signals:

The trigger for the cyclic data transmitting is selectable from two of a method, either an external timer signal to XTXTIM or the internal timer of MNM1221. The selection of trigger should be taken into the consideration of system structure. In general, it will be simple way to input the external timer signal because the synchronism with the NC operation is necessary for the timing. When selecting to use the internal timer, it will be necessary to synchronize the NC operation with the negative pulse output from XSYNC at the transmitting.

If not in RUNNING state or using the internal timer, XTXTIM input is ignored.

Also, XINTRX at completed receiving are outputted as timing signal to indicate to be able to access RX memory.

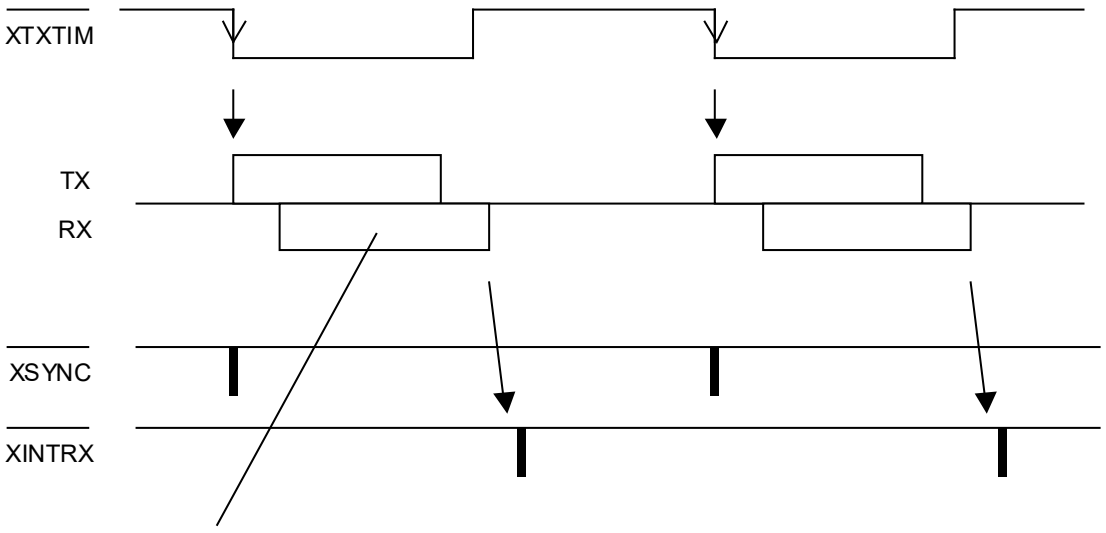


Note: The Low or High width of XTXTIM must keep minimum 1 us.

Basic Operation:

In running state, basically, when the command data written into TX memory is transmitted, the corresponding response data from Slaves will be received into RX memory.

Since the frame transmitting by Master makes Slave transmit the frame, the pair of TX and RX is corresponding as the physical frame. But note that the logical contents of the frame have time differential. Because there is no time that the firmware of Slave replies after interpreting the command in TX frame. Thus, as the logical contents, there is the response delay of at least one communication period. For example, an echo back data will be replied after one period. Particularly, the contents of the first RX frame must be ignored because there is no corresponding TX frame as logical.

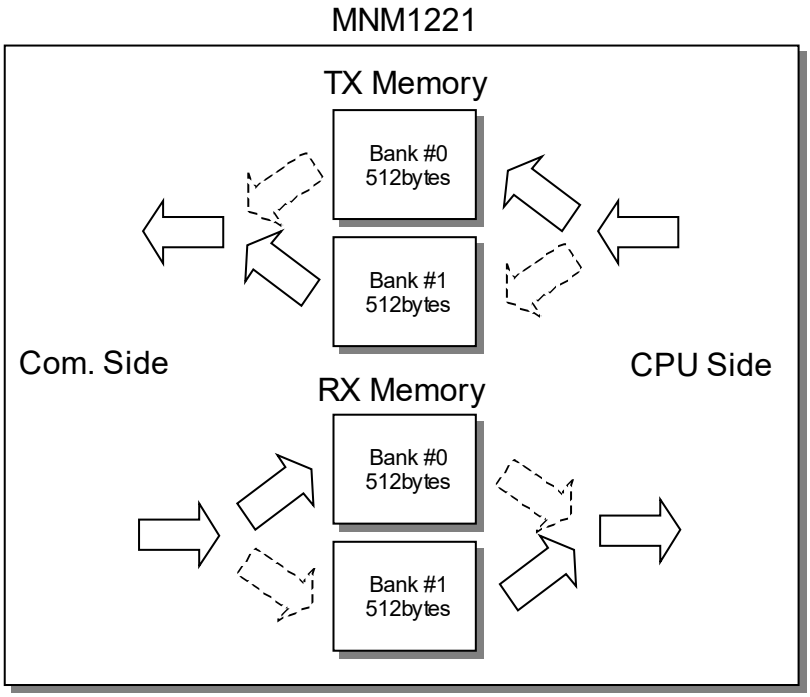


Note:

If RX frame is not received by the next transmitting timing, Timeout bit on M_ERR_FLAGS2 register will be set.

TX and RX Memory in MNM1221

A MNM1221 transmission buffer memory (TX memory) and reception buffer memory (RX memory) are respectively composed of 2 banks. To avoid conflict of data access, one bank is dedicated to the external CPU and another bank is dedicated to the internal communication module. And such assignment of the 2 banks is switched alternately.



Switching of banks:

	The trigger of switching	Deferred switching
TX memory	M_TXMEM_SW = 1 (This register is self cleared)	Being transmitted
RX memory	Receiving completion	M_RXMEM_HOLD = 1

Notes:

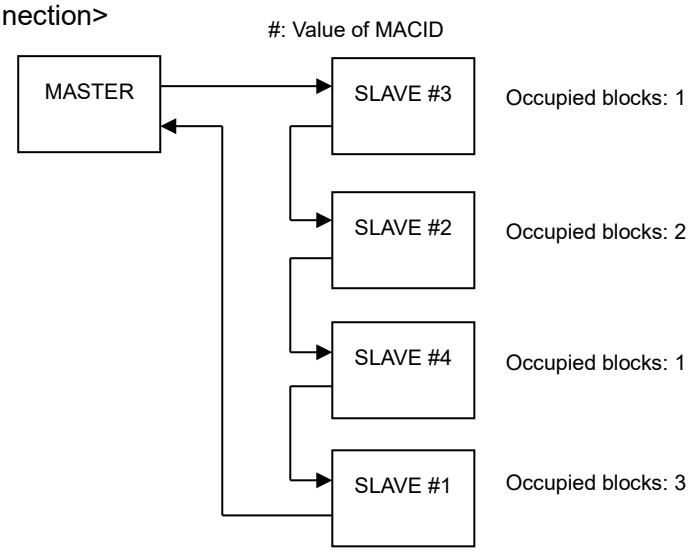
- For transmitting, M_ TXMEM_SW must be set to 1 after writing the data.
- At least once before reading the received data, M_RXMEM_HOLD must be set to 0 to allow switching the bank. While reading the data, M_RXMEM_HOLD must be set to 1 to prevent the switching.

Assignment on TX and RX Memory

The data of Slave nodes are arranged to on TX and RX memory in order of the cable connection. Since the arranging is from the lower block on the memory, the upper block area becomes empty if the sum of used blocks is less than 32.

The below figures show an example, there are Slave nodes that occupies plural blocks. But Slave normally occupies only one block.

<Structure of Connection>

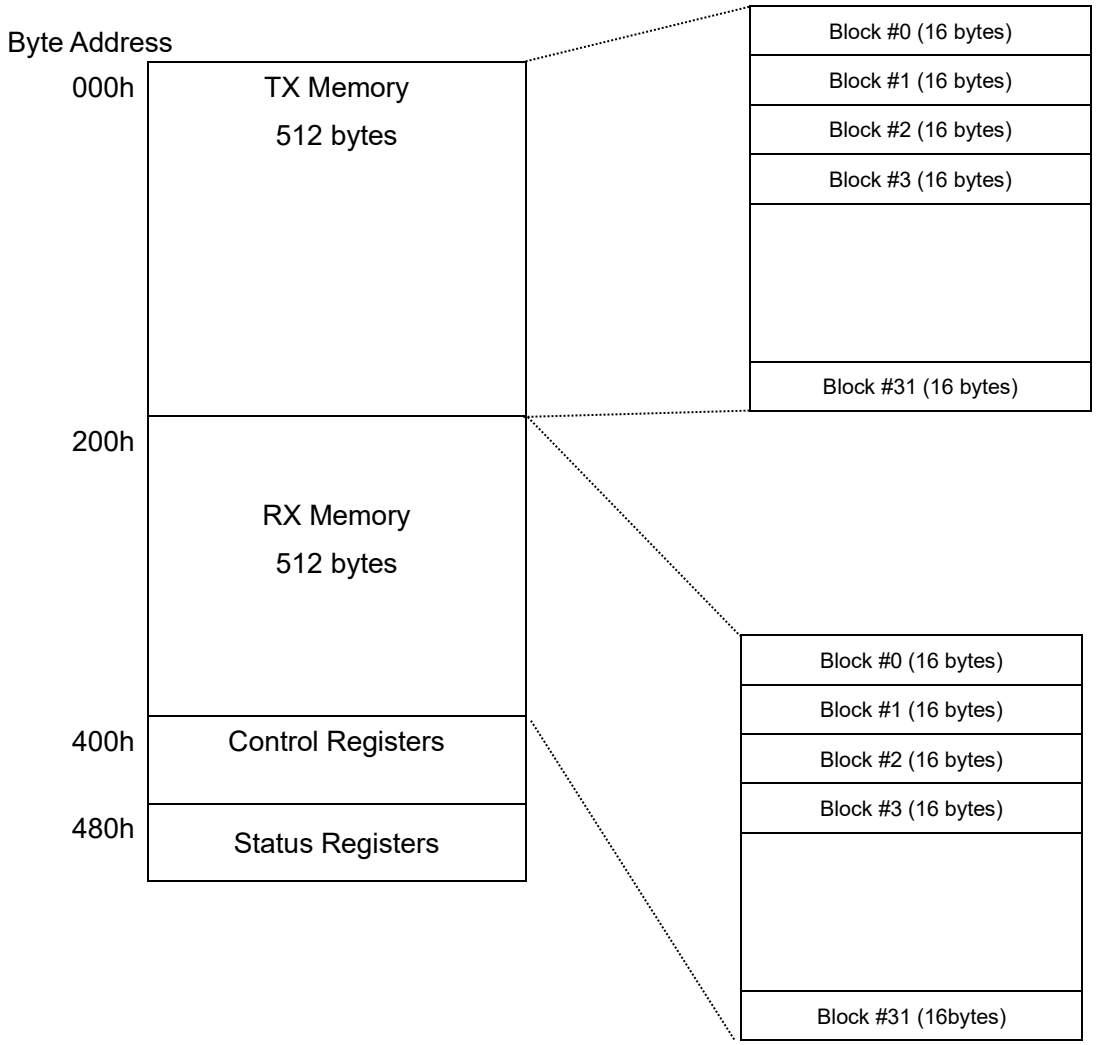


<Assignment on Memory>

Block #0	SLAVE #3
Block #1	SLAVE #2
Block #2	SLAVE #2
Block #3	SLAVE #4
Block #4	SLAVE #1
Block #5	SLAVE #1
Block #6	SLAVE #1
Block #7 to Block #31	Not used

Memory Map

Regardless of the bank switching, TX and RX memories are accessed with the same address.



Byte order:

“Little Endian” i.e. Lower data is in lower address.

Byte Address	4n + 3		4n + 2		4n + 1		4n + 0	
Data	31	24	23	16	15	8	7	0

(n: 0, 1, 2, 3, …)

Registers Description

Table of Registers

(1) Control Registers for Master

Address	Name	R/W	Default
400h	M_RESET	W	0000 0000h
404h	M_INITF_TX	R/W	0000 0000h
408h	M_CYCL_START	R/W	0000 0000h
414h	M_RTF_FORM	R/W	0000 0000h
418h	M_ERR_COUNT	R/W	0000 0333h
41Ch	M_INIT_DONE	R/W	0000 0000h
420h	M_TXTIM_SEL	R/W	0000 0000h
424h	M_TX_PERIOD	R/W	0000 C350h
458h	M_TXMEM_SW	R/W	0000 0000h
45Ch	M_RXMEM_HOLD	R/W	0000 0000h

(2) Status Registers for Master

Address	Name	R/W	Default
484h	M_STATE	R	0000 0008h
488h	M_INIT_ERR	R	0000 0000h
490h	M_ERR_FLAGS1	R	0000 0000h
494h	M_ERR_FLAGS2	R	0000 0000h
498h	M_DCRC_ERR	R	0000 0000h
49Ch	M_NODE_SUM	R	0000 0000h
4A0h	M_BLK_SUM	R	0000 0000h
4A4h	M_SINF_1_0	R	0000 0000h
4A8h	M_SINF_3_2	R	0000 0000h
4ACh	M_SINF_5_4	R	0000 0000h
4B0h	M_SINF_7_6	R	0000 0000h
4B4h	M_SINF_9_8	R	0000 0000h
4B8h	M_SINF_11_10	R	0000 0000h
4BCh	M_SINF_13_12	R	0000 0000h
4C0h	M_SINF_15_14	R	0000 0000h
4C4h	M_SINF_17_16	R	0000 0000h
4C8h	M_SINF_19_18	R	0000 0000h
4CCh	M_SINF_21_20	R	0000 0000h
4D0h	M_SINF_23_22	R	0000 0000h
4D4h	M_SINF_25_24	R	0000 0000h
4D8h	M_SINF_27_26	R	0000 0000h
4DCh	M_SINF_29_28	R	0000 0000h
4E0h	M_SINF_31_30	R	0000 0000h

Chip Reset

Address	Name	R/W	Default
400h	M_RESET	W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RST

Bit 0: RST

When this bit is set to 1, MNM1221 will be reset.

It is the same as Low input into XRST pin.

Immediately after writing 1 to this register, it enters the reset state, so other registers cannot be accessed subsequently. Wait at least 10 us before the next operation.

Bit 0	Description
0	No operate
1	Reset MNM1221 (Self clearing)

Initial Frame Transmit

Address	Name	R/W	Default
404h	M_INITF_TX	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	INF_TX

Bit 0: INF_TX

When this bit is set to 1, MNM1221 proceeds to RING CONFIG state.

Bit 0	Description
0	No operate
1	Transmit initial frame (Self clearing)

Cyclic Transmission Start

Address	Name	R/W	Default
408h	M_CYCL_START	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	CY_STA

Bit 0: CY_STA

When this bit is set to 1, MNM1221 proceeds to RUNNING state.

Bit 0	Description
0	No operate
1	Start cyclic transmission (Self clearing)

Real-Time Frame Format

Address	Name	R/W	Default
414h	M_RTF_FORM	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	FM1	FM0

Bit [1:0]: FM[1:0]

You must set both bit0 and bit1 to 1.

Bit1	Bit0	Description
0	0	For manufacturing test
0	1	
1	0	
1	1	Normal operation

Error Counter Setting

Address	Name	R/W	Default
418h	M_ERR_COUNT	R/W	0000 0333h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	Initial Error				Continuous Timeout				Continuous CRC ERR			

Normally this register is set to 0, because errors are detected by firmware without using these error counters.

Bit [11:8]: Initial Error

	Description
0	Disable the error counter. MNM1221 continues the ring configuration until pass successfully.
1 to 15	If initializing errors occur over the number of this value, MNM1221 stops the ring configuration, and goes to INITIAL state.

Bit [7:4]: Continuous Timeout

	Description
0	Disable the error counter. MNM1221 is in RUNNING state forever.
1 to 15	If continuous timeout in running state occurs over the number of this value, MNM1221 goes to INITIAL state.

Bit [3:0]: Continuous CRC ERR

	Description
0	Disable the error counter. The error flag is never set.
1 to 15	If continuous CRC error in running state occurs over the number of this value, MNM1221 set the error flag to 1.

Initializing Done

Address	Name	R/W	Default
41Ch	M_INIT_DONE	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	INI_DN

Bit 0: INI_DN

This bit must be set to 1 before M_INITF_TX register is set to 1.

Bit 0	Description
0	No operate
1	Set this bit to 1 after setting initial registers.

Transmit Timing Select

Address	Name	R/W	Default
420h	M_TXTIM_SEL	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TM_SEL

Bit 0: TM_SEL

Select timing clock for transmit in RUNNING state.

Bit 0	Description
0	Internal timer
1	External clock into XTXTIM pin.

Transmission Period

Address	Name	R/W	Default
424h	M_TX_PERIOD	R/W	0000 C350h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Transmission Period															

Bit [15:0]: Transmission Period

Set transmission period in RUNNING state when using internal timer.

Period = 40[ns] x setting value

e.g.)

Period	Setting value
1000 us	61A8h
500 us	30D4h
250 us	186Ah
125 us	0C35h

Notes:

- The period cannot be set up freely because it must be synchronized with the servo control on Slave side. Refer to “Transmission in RUNNING state”.
- It is not possible to set a period of 62.5 us to the internal timer, so in that case, use an external timer.

Transmission Memory Switch

Address	Name	R/W	Default
458h	M_TXMEM_SW	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TXM_SW

Bit 0: TXM_SW

Switch transmission memory bank.

For transmission, this bit must be set to 1 after writing TX memory.

Bit 0	Description
0	No operate
1	Switch TX memory bank (Self clearing)

Receiving Memory Hold

Address	Name	R/W	Default
45Ch	M_RXMEM_HOLD	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RXM_HD

Bit 0: RXM_HD

While this bit is set to 1, receiving memory bank is not switched. If received in such a period, the switching is deferred until clearing to 0.

Bit 0	Description
0	Enable switching RX memory bank
1	Hold RX memory bank

Communication State

Address	Name	R/W	Default
484h	M_STATE	R	0000 0008h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frame ID								-	-	-	-	State			

Bit [15:8]: Frame ID

Indicates the Frame ID in the received frame.

Bit [3:0]: State

Indicates the MNM1221 state.

Bit3	Bit2	Bit1	Bit0	State
1	0	0	0	INITIAL
0	1	0	0	RING CONFIG
0	0	1	0	READY
0	0	0	1	RUNNING
Else				None

Initializing Error

Address	Name	R/W	Default
488h	M_INIT_ERR	R	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	INI_ER

Bit0: INI_ER

When errors are detected over the number of the Initial error field in M_ERR_COUNT register at ring configuration, this bit becomes 1.

Bit 0	Description
0	Normal state
1	Initializing error (Latched and Cleared after read)

Error Flags 1 (Errors at RING CONFIG)

Address	Name	R/W	Default
490h	M_ERR_FLAGS1	R	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Error Flags 1															

This register indicates errors at RING CONGIF state.

When an error is detected, each bit is latched to 1. After reading, it is cleared to 0.

Bit15: Init-B frame CRC-error 2

If the Error Marking in the Init-B frame indicates an error, this bit becomes 1.

Bit14: Init-B frame CRC-error 1

If the Frame CRC in the Init-B frame indicates an error, this bit becomes 1.

Bit13: Init-B frame ACK mismatch

If there is a slave that does not respond to the Init-B frame, this bit becomes 1.

Bit12: Init-B frame length short

If the length of the Init-B frame is short, this bit becomes 1.

Bit11: Not used

Ignore this bit.

Bit10: Init-B frame ID error

If the Frame ID in the Init-B frame indicates an error, this bit becomes 1.

Bit9: Init-B frame ID mismatch

If the Frame IDs do not match between sending and receiving the Init-B frames, this bit becomes 1.

When this bit is 1, Bit10 is also 1.

Bit8: Init-B frame timeout

If the Init-B frame is not received within 2 ms after sending it, this bit becomes 1.

Bit7: Init-A frame CRC-error 2

If the Error Marking in the Init-A frame indicates an error, this bit becomes 1.

Bit6: Init-A frame CRC-error 1

If the Frame CRC in the Init-A frame indicates an error, this bit becomes 1.

Bit5: Init-A frame length short

If the length of the Init-A frame is short, this bit becomes 1.

Bit4: Init-A frame block sum error

If the sum of blocks is 0 or over 32, this bit becomes 1.

Bit3: Init-A frame node sum error

If the sum of nodes is 0 or over 32, this bit becomes 1.

Bit2: Init-A frame ID error

If the Frame ID in the Init-A frame indicates an error, this bit becomes 1.

Bit1: Init-A frame ID mismatch

If the Frame IDs do not match between sending and receiving the Init-A frames, this bit becomes 1. When this bit is 1, Bit2 is also 1.

Bit0: Init-A frame ID timeout

If the Init-A frame is not received within 2 ms after sending it, this bit becomes 1.

Note:

When any of Bit12, Bit[10:8], Bit5, or Bit[2:0] is 1, MNM1221 does not output XINTRX.

If reading this register in an interrupt by XINTRX, these bits indicate the previous error.

Error Flags 2 (Errors at RUNNING)

Address	Name	R/W	Default
494h	M_ERR_FLAGS2	R	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	Error Flags 2													

This register indicates errors at RUNNING state.

When an error is detected, each bit except Bit11 is latched to 1. After reading, it is cleared to 0.

For decision whether received data is ok, M_DCRC_ERR should be used instead of this register.

Bit13: Frame length short

If the length of the frame is short, this bit becomes 1.

Bit12: MII RXER

If both RXER and RXDV of MII are “H”, this bit becomes 1.

Bit11: Real-time frame Data-CRC-error (OR of bits in M_DCRC_ERR register)

This bit is simply “OR” of all bits in M_DCRC_ERR, so, not latched and not cleared after reading.

Bit10: Real-time frame continuous CRC-error

The condition of this bit set is defined M_ERR_COUNT register.

Bit9: Real-time frame CRC-error 2

If the Error Marking in the Real-time frame indicates an error, this bit becomes 1.

Bit8: Init-C frame CRC-error 2

Reserved (Always 0)

Bit7: Init-B frame CRC-error 2

Reserved (Always 0)

Bit6: Real-time frame CRC-error 1

If the Frame CRC in the Real-time frame indicates an error, this bit becomes 1.

Bit5: Init-C frame CRC-error 1

Reserved (Always 0)

Bit4: Init-B frame CRC-error 1

Reserved (Always 0)

Bit3: Frame ID mismatch

If the Frame IDs do not match between sending and receiving frames, this bit becomes 1.

When this bit is 1, Bit2 is also 1.

Bit2: Frame ID error

If the Frame ID in the frame indicates an error, this bit becomes 1.

Bit1: Continuous timeout

The condition of this bit set is defined M_ERR_COUNT register.

If this bit becomes 1, MNM1221 go to INITIAL state.

Bit0: Timeout

If RX not coming until the next TX timing, this bit becomes 1.

Note:

When any of Bit13, Bit3, Bit2, or Bit0 is 1, MNM1221 does not output XINTRX.

If reading this register in an interrupt by XINTRX, these bits indicate the previous error.

Data CRC Errors

Address	Name	R/W	Default
498h	M_DCRC_ERR	R	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
#31	#30	#29	#28	#27	#26	#25	#24	#23	#22	#21	#20	#19	#18	#17	#16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
#15	#14	#13	#12	#11	#10	#9	#8	#7	#6	#5	#4	#3	#2	#1	#0

Bit n: #n

When Data CRC errors is detected in the block at RUNNING state, this bit becomes 1.

The bit number corresponds to the block number.

Normally, this register is used for decision whether received data is OK, and M_ERR_FLAGS2 is not used. Because there is the case that M_ERR_FLAGS2 shows errors but M_DCRC_ERR shows no errors by error correcting function of MNM1221. In such a case, the data can be used.

	Description
0	Normal state
1	CRC error of data block (Latched and Cleared after read)

Slave Node Sum

Address	Name	R/W	Default
49Ch	M_NODE_SUM	R	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	Slave Node Sum							

Bit [7:0]: Slave Node Sum

Indicates the sum of Slave nodes detected in RING CONFIG state.

Data Block Sum

Address	Name	R/W	Default
4A0h	M_BLK_SUM	R	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	Data Block Sum										

Bit [10:0]: Data Block Sum

Indicates the sum of Slave data blocks detected in RING CONFIG state.

Slave Information

Address	Name	R/W	Default
4A4h	M_SINF_1_0	R	0000 0000h
4A8h	M_SINF_3_2	R	0000 0000h
4ACh	M_SINF_5_4	R	0000 0000h
4B0h	M_SINF_7_6	R	0000 0000h
4B4h	M_SINF_9_8	R	0000 0000h
4B8h	M_SINF_11_10	R	0000 0000h
4BCh	M_SINF_13_12	R	0000 0000h
4C0h	M_SINF_15_14	R	0000 0000h
4C4h	M_SINF_17_16	R	0000 0000h
4C8h	M_SINF_19_18	R	0000 0000h
4CCh	M_SINF_21_20	R	0000 0000h
4D0h	M_SINF_23_22	R	0000 0000h
4D4h	M_SINF_25_24	R	0000 0000h
4D8h	M_SINF_27_26	R	0000 0000h
4DCh	M_SINF_29_28	R	0000 0000h
4E0h	M_SINF_31_30	R	0000 0000h

Bit fields:

Bit [31:16] is for Slave#2n+1

Bit [15:0] is for Slave#2n

(n: 0, 1, 2, … 15)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ACT	MODE[1:0]		MAC-ID					-	-	Number of Blocks					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACT	MODE[1:0]		MAC-ID					-	-	Number of Blocks					

This register indicates the Slave information detected in RING CONFIG state.

Bit 31, Bit 15: ACT

Indicates presence of the Slave node.

	Description
0	Not detected
1	Presence (The Slave is active.)

Bit [30:29], Bit [14:13]: MODE[1:0]

Indicates a kind of the Slave node.

MODE1	MODE0	Description
0	0	None
0	1	Generic slave
1	0	Input slave
1	1	Output slave

Bit [28:24], Bit [12:8]: MAC-ID (Node Address)

Indicates MAC-ID (0 to 31) of the Slave node.

Using this information, duplicate MAC-ID checking by firmware is needed before proceeding to RUNNING state.

Bit [21:16], Bit [5:0]: Number of Blocks

Indicates the number of data blocks the Slave node occupies.

MII Register Access

MNM1221 provides registers to access MII registers inside PHY chip.
In most PHY, this register access is not necessary since MNM1221 can perform properly with pin configuration only. But, some PHY such as KSZ8041 by Micrel needs the MII register setting as well. For the access, MDIO and MDC signals are used. See the following figure.

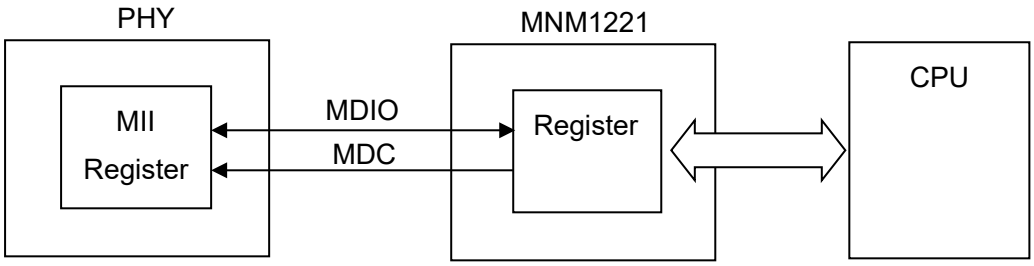


Table of Registers

(1) Control Registers

Address	Name	R/W	Default
448h	M_MDIO_WDAT	R/W	0000 0000h
44Ch	M_MDIO_ADDR	R/W	0000 0020h
450h	M_MDIO_WR	R/W	0000 0000h
454h	M_MDIO_RD	R/W	0000 0000h

(2) Status Register

Address	Name	R/W	Default
4F8h	M_MDIO_RDAT	R	0000 0000h

MDIO Write Data

Address	Name	R/W	Default
448h	M_MDIO_WDAT	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write Data															

Bit [15:0]: Write Data

Set the data written into the MII register.

Note:
In the following time period, do not write any data into this register to perform proper operation.

- While M_MDIO_WR register shows 1 (in writing)
- 5 us after M_MDIO_WR register changed from 1 to 0
- While M_MDIO_RD register shows 1 (in reading)
- 5 us after M_MDIO_RD register changed from 1 to 0

MDIO Address

Address	Name	R/W	Default
44Ch	M_MDIO_ADDR	R/W	0000 0020h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	PHY Address					Register Address				

Bit [9:5]: PHY Address

Set the address of PHY chip.

Bit [9:5]: Register Address

Set the address of MII register inside PHY chip.

Note:

In the following time period, do not write any data into this register to perform proper operation.

- While M_MDIO_WR register shows 1 (in writing)
- 5 us after M_MDIO_WR register changed from 1 to 0
- While M_MDIO_RD register shows 1 (in reading)
- 5 us after M_MDIO_RD register changed from 1 to 0

MDIO Write Command

Address	Name	R/W	Default
450h	M_MDIO_WR	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	WR

Bit 0: WR

When this bit is set to 1 after setting the M_MDIO_WDAT and M_MDIO_ADDR register, MII register writing will be started. After writing is completed, this bit returns to 0 automatically.

Bit 0	Description
0	Invalid
1	Writing (After writing, 0 cleared automatically)

Writing time for MII register: approximately 82 us

Note:

In the following time period, do not write any data into this register to perform proper operation.

- While M_MDIO_WR register shows 1 (in writing)
- 5 us after M_MDIO_WR register changed from 1 to 0
- While M_MDIO_RD register shows 1 (in reading)
- 5 us after M_MDIO_RD register changed from 1 to 0

MDIO Read Command

Address	Name	R/W	Default
454h	M_MDIO_RD	R/W	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RD

Bit 0: RD

When this bit is set to 1 after setting the M_MDIO_ADDR register, readout data from MII register will be stored to M_MDIO_RDAT register. After reading is completed, this bit returns to 0 automatically.

Bit 0	Description
0	Invalid
1	Reading (After reading, 0 cleared automatically)

Reading time for MII register: approximately 82 us

Note:

In the following time period, do not write any data into this register to perform proper operation.

- While M_MDIO_WR register shows 1 (in writing)
- 5us after M_MDIO_WR register changed from 1 to 0
- While M_MDIO_RD register shows 1 (in reading)
- 5us after M_MDIO_RD register changed from 1 to 0

MDIO Read Data

Address	Name	R/W	Default
4F8h	M_MDIO_RDAT	R	0000 0000h

Bit fields:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Data															

Bit [15:0]: Read Data

Readout data from MII register is stored.

Note:
In the following time period, do not access this register to prevent invalid reading.

- While M_MDIO_WR register shows 1 (in writing)
- 5 us after M_MDIO_WR register changed from 1 to 0
- While M_MDIO_RD register shows 1 (in reading)
- 5 us after M_MDIO_RD register changed from 1 to 0

Chapter 3
Slave Operation

Overview

Introduction

This chapter is to describe slave function of MNM1221. The same functions as in master are omitted.

Features in Slave

- Three slave modes of Generic, IN (32 points) and OUT (32 points)
- XSYNC output pin for synchronized control
- 16 or 8-bit width of data bus in Generic slave mode
- CPU no need on IN or OUT slave

< Functional Comparison >

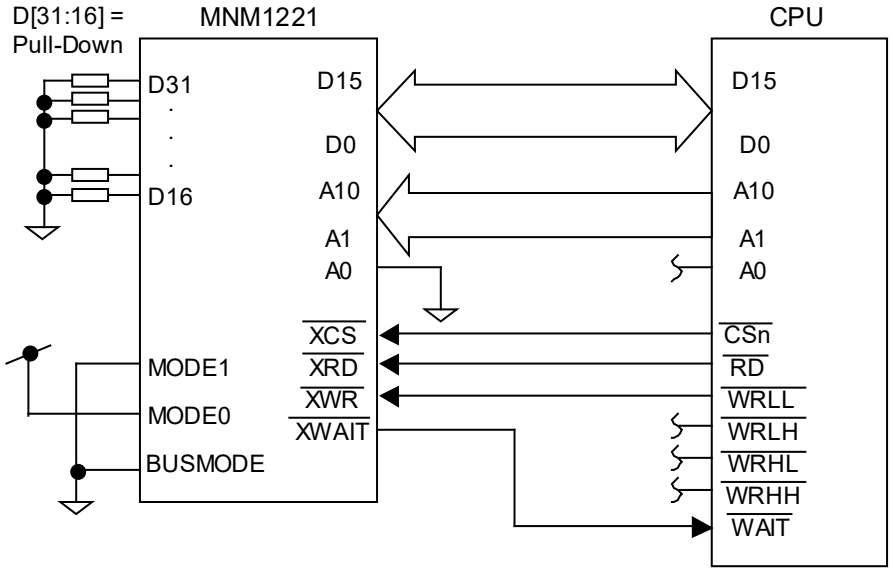
	Master	**Slave**	
		Generic (Note)	**IN / OUT**
CPU	Need	Need	No Need
Data Pins	Data Bus （32 or 16-bit）	Data Bus （16 or 8-bit）	Input or Output Pins （32）
Address Pins	Address Bus	Address Bus	MAC-ID Setting
Pin91	XWAIT	XWAIT	XLED
Trigger of Transmitting	Internal Timer or XTXTIM input	Receiving Frame	Receiving Frame
XSYNC Output Timing	Transmitting	After All Slaves Receiving (RUNNING State Only)	After All Slaves Receiving (RUNNING State Only)
Conditions of Timeout Detection	No Receiving before the Next Transmitting	No Receiving for a Certain Time Set with Register	No Receiving for a Certain Time (20.9 ms Fixed)

Note: “Generic” mode can be used for various applications also including in/out device.

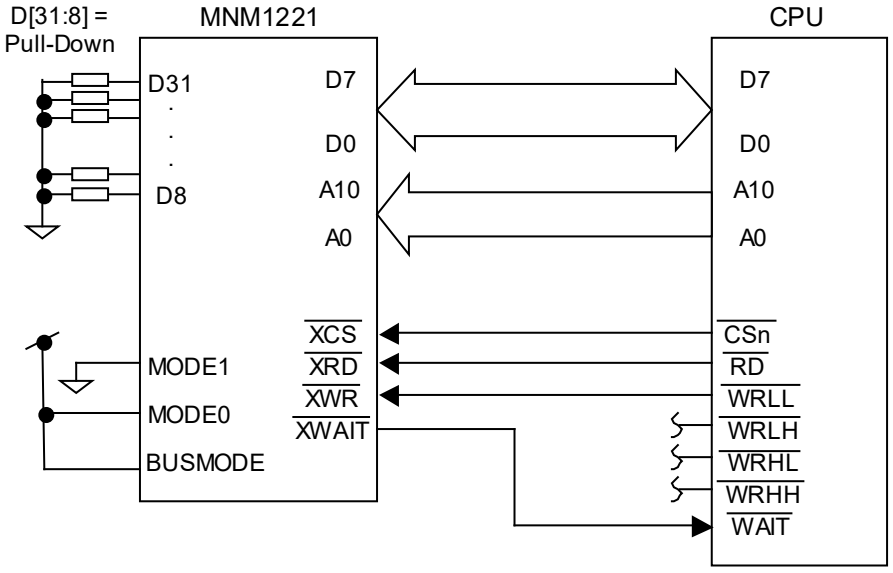
Connection for Slave

Bus Interface with CPU in Generic slave

16bit bus (BUSMODE = L):



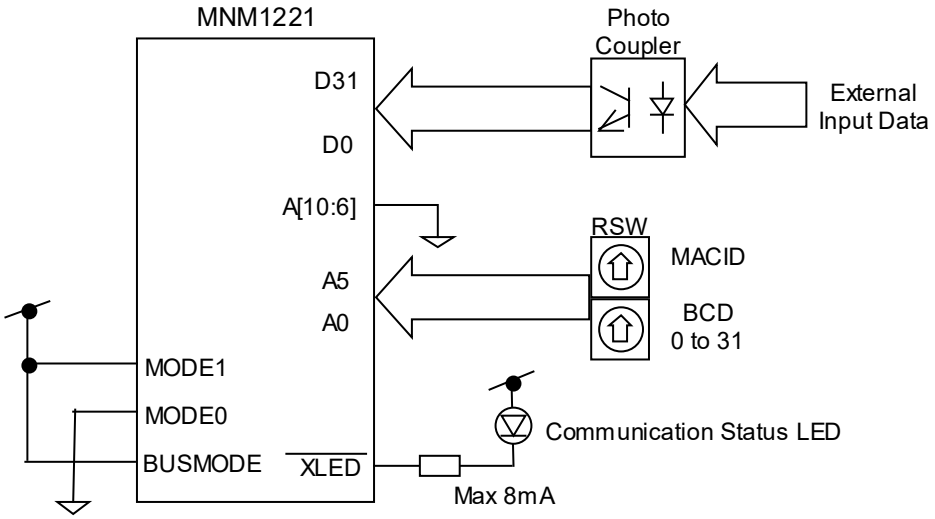
8bit bus (BUSMODE = H):



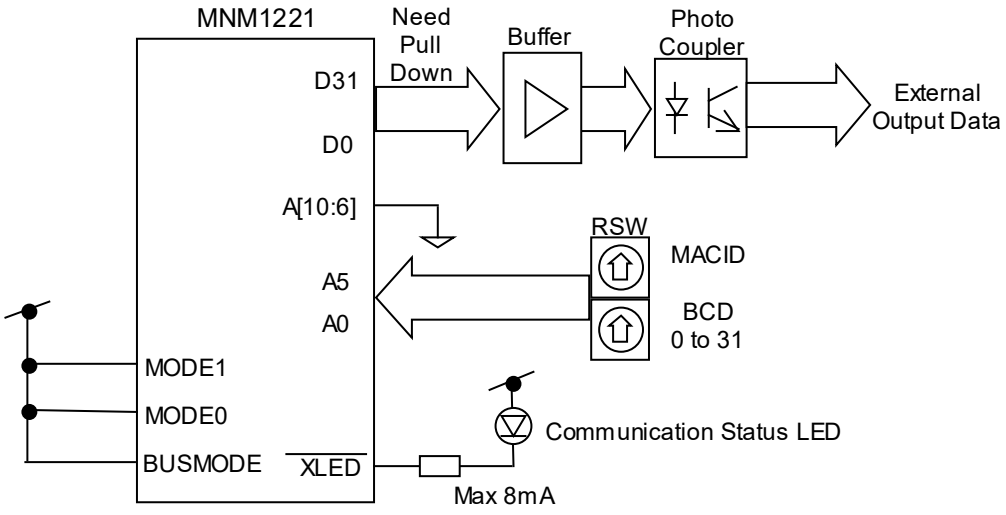
Note: For pull-down resistor for unused data-bus, about 10 k Ohm is recommended.

The above figure shows an example of CPU with byte-unit address bus

Connection for IN slave



Connection for OUT slave



Note:

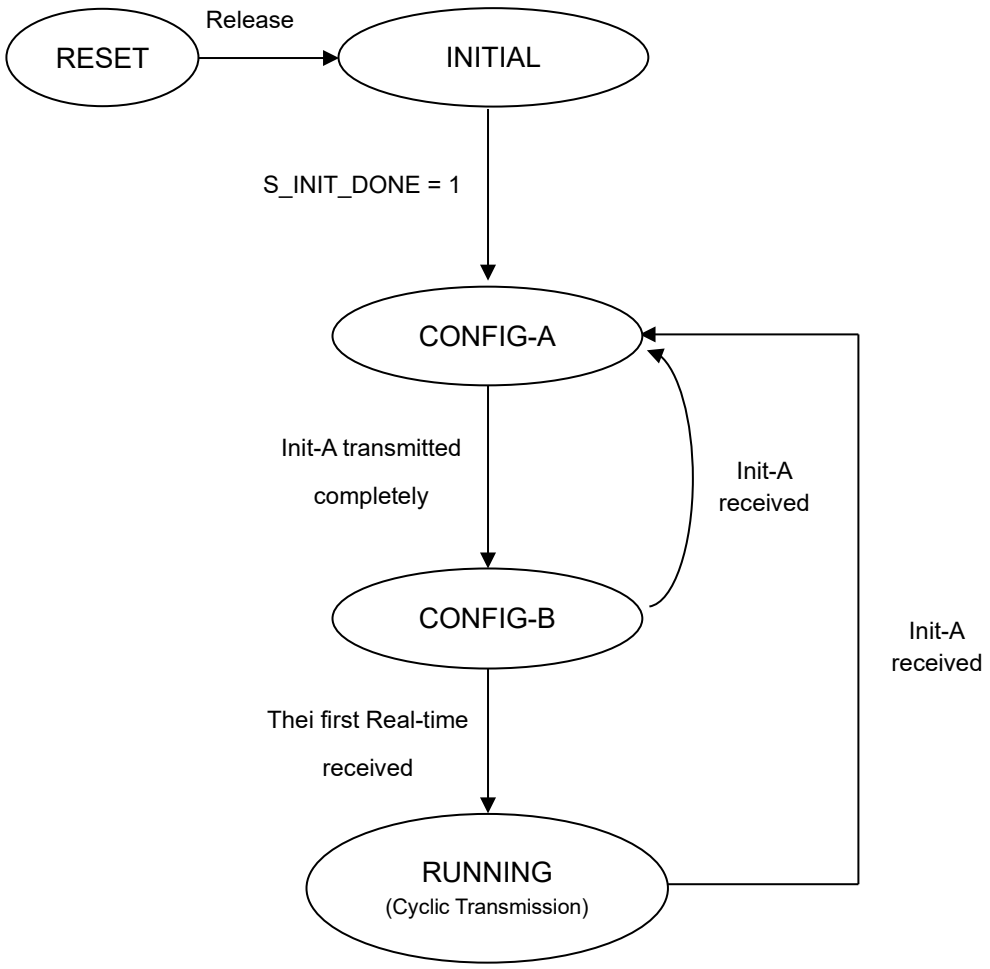
When MAC-ID is used for BCD input (BUSMODE: H) such as the above figure, unsuitable value, e.g. more than 31 or Ah to Fh of lower 4bit, is used as 31.

Functional Description

State Transition of MNM1221

The following figure shows the state transition from RESET to RUNNING which performs cyclic transmission.

"S_…": control registers



Note:

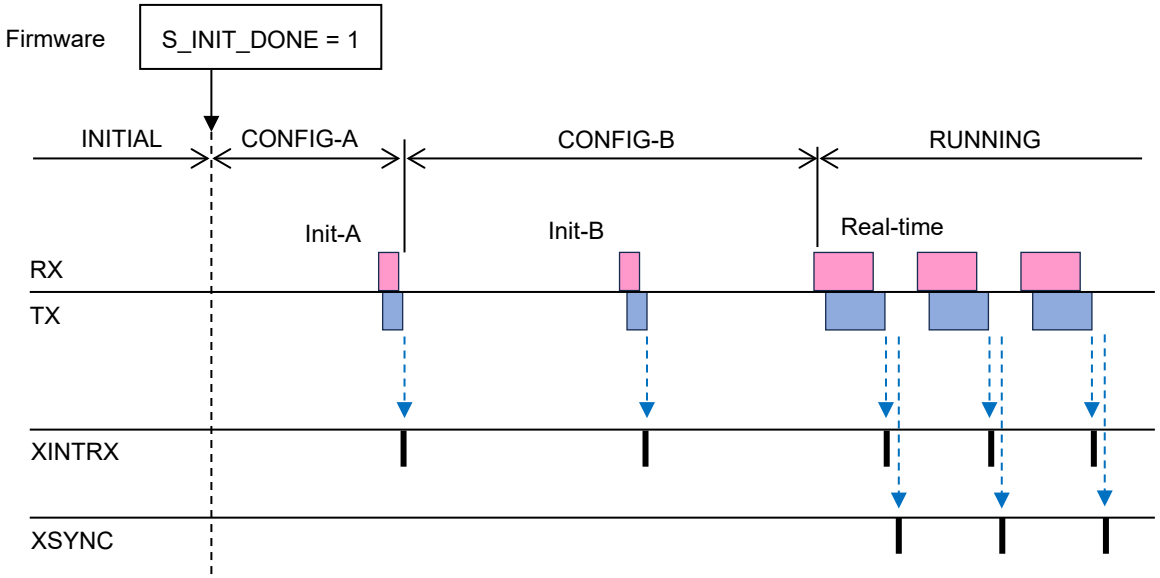
Though not indicated in the above figure, if S_RESET register is set to 1, the state goes to INITIAL from any state.

Descriptions of Each State

State	Descriptions	Valid Frame
INITIAL	Each MNM1221 register is initialized with the firmware after reset. When S_INIT_DONE register is set to 1 after initializing, the state goes to CONFIG-A and the receiving is enabled. In IN/OUT slave, the state automatically goes to CONFIG-A. In addition, any frame received in INITIAL state is ignored.	-
CONFIG-A	Init-A frame from master is received and the frame added my node information is transmitted. After that, the state goes to CONFIG-B. Any frame other than Init-A is ignored. This process is automatically done by MNM1221.	Init-A
CONFIG-B	Init-B frame from master is received and the frame added my node information is transmitted. After that, when receiving the first Real-time frame, the state goes to RUNNING. If init-A frame is received, the state goes to CONFIG-A. The other frame is ignored. This process is automatically done by MNM1221. After this CONFIG-B state, the location of my data block in RX memory is fixed.	Init-B Init-A
RUNNING	The cyclic transmission is done with Real-time frame. The firmware exchanges the data with TX/RX memory in MNM1221. If init-A frame is received, the state goes to CONFIG-A. The other frame is ignored.	Real-time Init-A

Note:
Except for the transition from INITIAL to CONFIG-A, the correspondence between receiving and transmitting (replying) causes the transition. Therefore, the master operation makes the slave transit the state.

Time Chart at Start-up



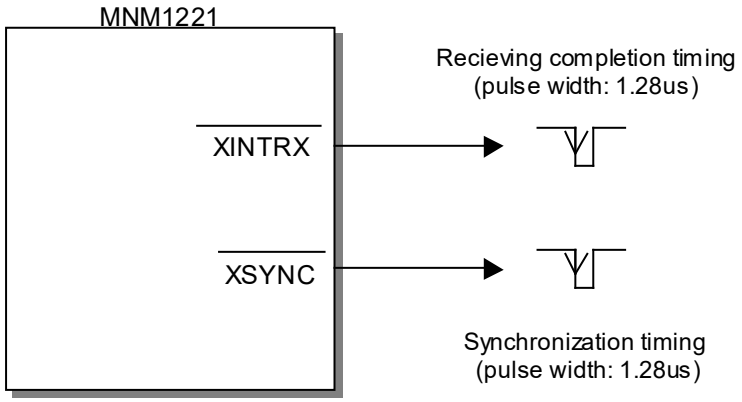
Note:

XSYNC is outputted in RUNNING state only. This function is different from master.

Timing Signal Output

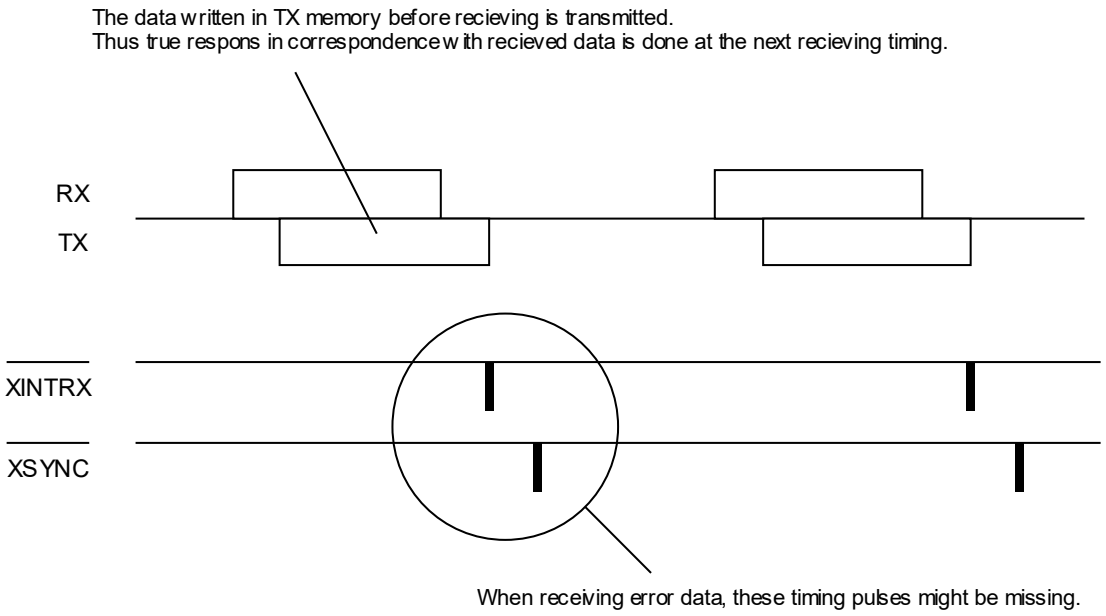
There are two signals, XINTRX is outputted at receiving the frame, and XSYNC is used for the timing reference of control in RUNNING state. In both signals, falling edge is effective and the pulse width is 1.28us. Note that XSYNC is outputted in RUNNING state only.

	XINTRX	XSYNC
Output Conditions	It is outputted at receiving the frame completely independent of the state or type of the frame. In RUNNING state, if the timeout is detected, it is also outputted. In this case, the output can be masked with setting the register.	In RUNNING state, it is outputted at the same time of all slaves after receiving the Real-time frame completely. In IN/OUT slave, at this signal timing, the data sampling or outputting is done.
Remark		Synchronized with this signal, received command data should be read and reflected in the motor control. Thus the motions of all axes will be synchronized.



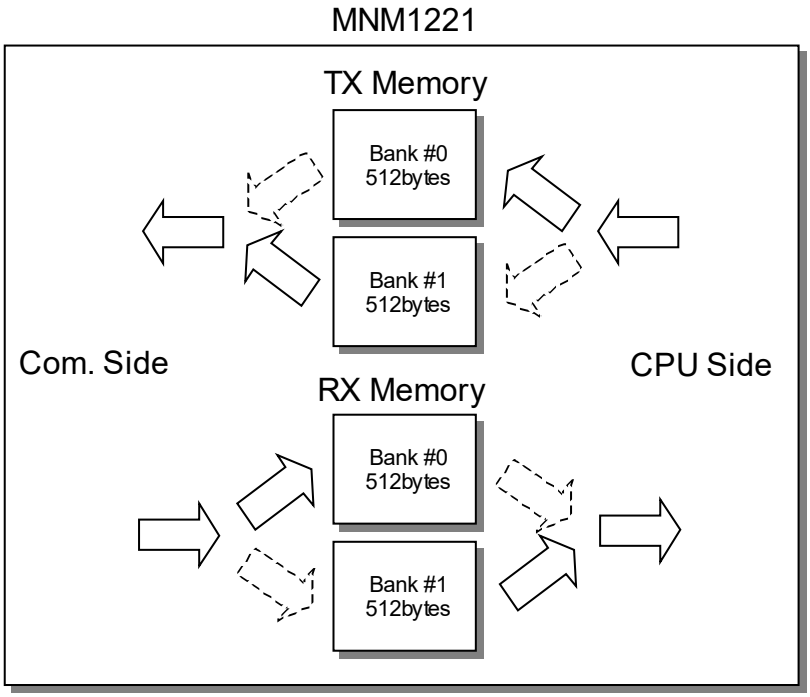
Transmission in RUNNING state

In slave, receiving triggers off transmitting. MNM1221 transmits the data written in TX memory before receiving. Therefore, even if the corresponding response data is written in TX memory immediately after receiving, its transmitting is delayed until the next receiving timing. That means the receiving and transmitting physical frames are always corresponding, however, the contents of the two frames are not corresponding and there is a delay of at least one cycle.
Even if an error is detected in the received data, the transmitting is basically done. However there are cases where the transmitting cannot be done according to the error. In this case, the same operation as non-receiving is performed, the receiving data is not stored into RX memory, and the timing pulses of XINTRX and XSYNC are not outputted. Since the receiving on the cycle is missing, the firmware process never causing a problem in this case must be done.



TX and RX Memory in MNM1221

MNM1221 transmission buffer memory (TX memory) and reception buffer memory (RX memory) are respectively composed of 2 banks. To avoid conflict of data access, one bank is dedicated to the external CPU and another bank is dedicated to the internal communication module. And such assignment of the 2 banks is switched alternately. This memory structure is the same as master.



Switching of banks:

	Trigger of switching	Deferred switching
TX memory	S_TXMEM_SW = 1 (This register is self cleared)	In transmitting
RX memory	Receiving completion	S_RXMEM_HOLD = 1

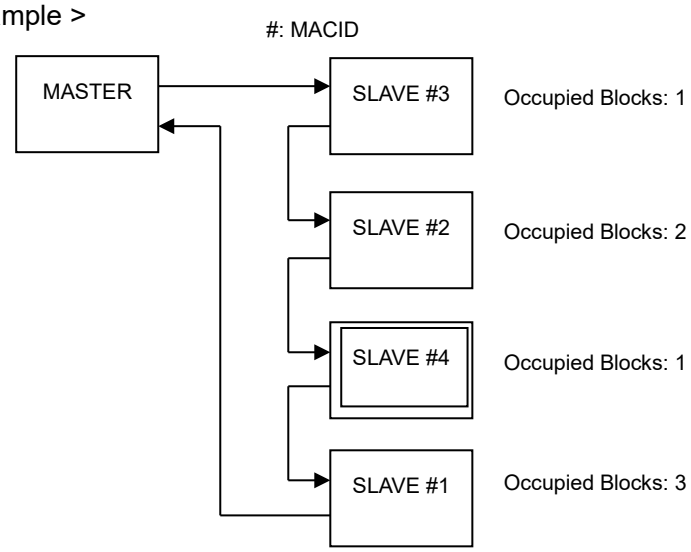
Notes:

- For transmitting, S_ TXMEM_SW must be set to 1 after writing the data.
- At least once before reading the received data, S_RXMEM_HOLD must be set to 0 to allow switching the bank. If the reading does not conflict with receiving such as the system which reads immediately after receiving completion, S_RXMEM_HOLD should be set to always 0 (enable switching). If the conflict might occur, while reading the data, S_RXMEM_HOLD must be set to 1 to prevent the switching.

Location in TX and RX Memory

In receiving, the data of all slaves is assigned into the RX memory in order of the cable connection like master. Before accessing the RX memory, it is necessary to check my node location with looking at S_BLK_ORDER register. In transmitting, the data of my node must be written from the beginning (block #0) in the TX memory regardless of the connection order. Therefore the data location is different between receiving and transmitting.

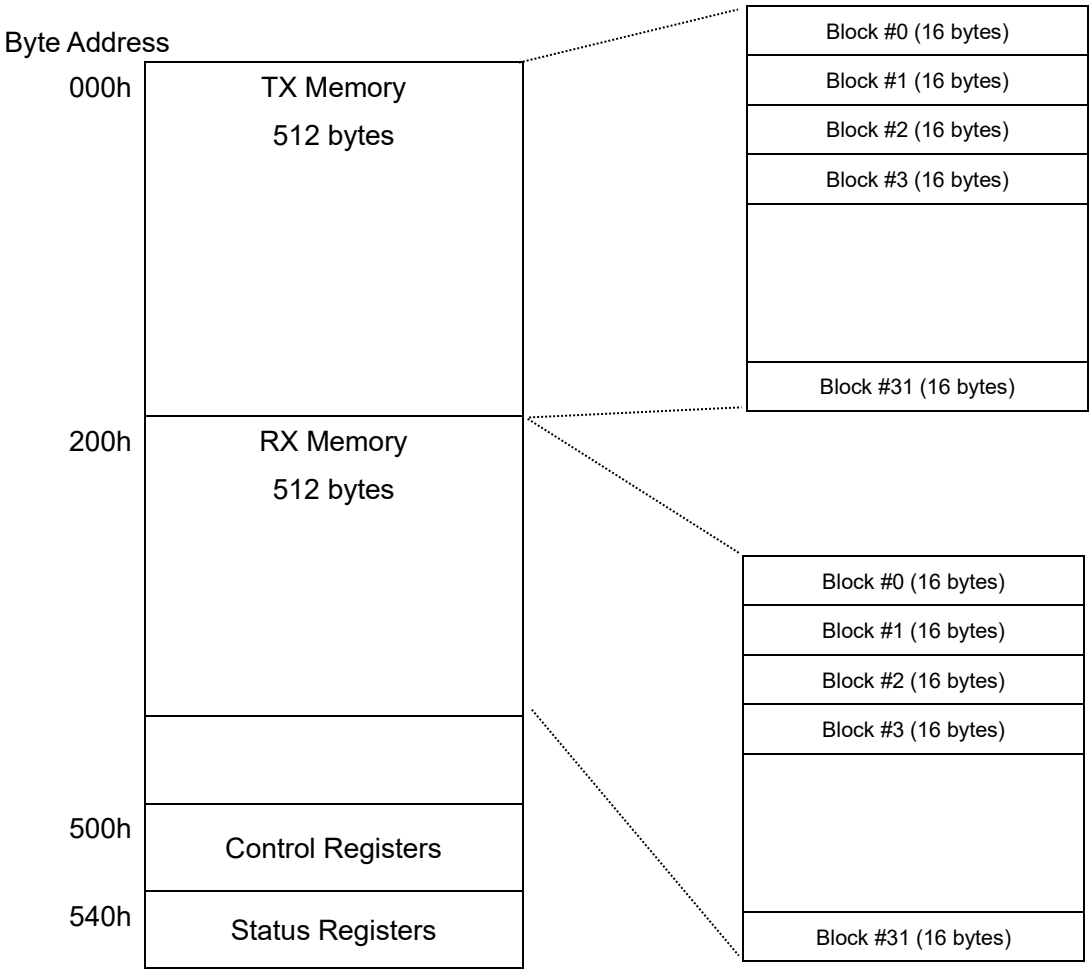
< Connection Example >



< Location of SLAVE#4 >

	RX Memory	TX Memory
Block #0	SLAVE #3	SLAVE #4
Block #1	SLAVE #2	Not used
Block #2	SLAVE #2	Not used
Block #3	SLAVE #4	Not used
Block #4	SLAVE #1	Not used
Block #5	SLAVE #1	Not used
Block #6	SLAVE #1	Not used
Block #7 to Block #31	Not used	Not used

Memory Map



Byte order:

“Little Endian” i.e. Lower data is in lower address.

Byte Address	4n + 3		4n + 2		4n + 1		4n + 0	
Data	31	24	23	16	15	8	7	0

(n: 0, 1, 2, 3, …)

Registers Description

Table of Registers

(1) Control Registers for Slave

Address	Name	R/W	Default
500h	S_RESET	W	0000h
504h	S_MACID	R/W	0000h
508h	S_BLK_N	R/W	0001h
50Ch	S_TIMEOUT	R/W	00FFh
510h	S_INIT_DONE	R/W	0000h
514h	S_INTRX_MSK	R/W	0000h
518h	S_SYNC_DELAY	R/W	0000h
51Ch	S_SYNC_MSK	R/W	0000h
530h	S_TXMEM_SW	R/W	0000h
534h	S_RXMEM_HOLD	R/W	0000h

(2) Status Registers for Slave

Address	Name	R/W	Default
544h	S_STATE	R	0008h
548h	S_OVER_N	R	0000h
54Ch	S_ERR_FLAGS	R	0000h
550h	S_DCRC_ERR_L	R	0000h
554h	S_DCRC_ERR_H	R	0000h
558h	S_NODE_ORDER	R	0000h
55Ch	S_BLK_ORDER	R	0000h
560h	S_NODE_SUM	R	0000h
564h	S_BLK_SUM	R	0000h

Chip Reset

Address	Name	R/W	Default
500h	S_RESET	W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RST

Bit 0: RST

When this bit is set to 1, MNM1221 will be reset.

It is the same as Low input into XRST pin.

Immediately after writing 1 to this register, it enters the reset state, so other registers cannot be accessed subsequently. Wait at least 10 us before the next operation.

Bit 0	Description
0	No operate
1	Reset MNM1221 (Self clearing)

MAC-ID Setting

Address	Name	R/W	Default
504h	S_MACID	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	MAC-ID				

Bit [4:0]: MAC-ID

MAC-ID value (0 to 31) of my node must be set.

MAC-ID is the same as Node Address.

Number of Occupied Blocks

Address	Name	R/W	Default
508h	S_BLK_N	R/W	0001h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	BLK_N					

Bit [5:0]: BLK_N

The number of blocks my node occupies must be set.

The setting range is 1 to 32. If unsuitable value is input, the operation is not guaranteed.

Timeout Setting

Address	Name	R/W	Default
50Ch	S_TIMEOUT	R/W	00FFh

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	TIMEOUT							

Bit [7:0]: TIMEOUT

Timeout detection in RUNNING state is set.

When 0 is set, the detection is disabled. If in the other way timeout is detected, set 0.

Value	Description
0	Disable timeout detection.
Else	Enable timeout detection. Detection time = 81.92 us x (setting value)

Initializing Done

Address	Name	R/W	Default
510h	S_INIT_DONE	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	INI_DN

Bit 0: INI_DN

After initial setting of each register, this bit must be set to 1.

With this operation, the state goes from INITIAL to CONFIG-A which enables receiving the frame.

During 0 of this bit, frames are ignored.

Bit 0	Description
0	No operate
1	Enable receiving.

INTRX Mask at Timeout

Address	Name	R/W	Default
514h	S_INTRX_MSK	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	IRX_MK

Bit 0: IRX_MK

XINTRX is outputted at detected timeout as well as receiving the frame. When this bit is set to 1, the output by timeout is masked.

Bit 0	Description
0	At both receiving frame and detected timeout, XINTRX is outputted.
1	Only at receiving frame, XINTRX is outputted.

SYNC Output Delay

Address	Name	R/W	Default
518h	S_SYNC_DELAY	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	SYNC_DELAY						

Bit [6:0]: SYNC_DELAY

Additional delay time for XSYNC output is set. This setting is applied to my node, and is not effective in the other nodes. Normally, set to 0 (no delay).

Value	Description
0	No delay
Else	Delay time = 0.64 us x (setting value)

SYNC Output Mask

Address	Name	R/W	Default
51Ch	S_SYNC_MSK	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SYN_MK

Bit 0: SYN_MK

If it is needed to mask the XSYNC output, set this bit to 1.

Bit 0	Description
0	Enable XSYNC output
1	Disable XSYNC output

Transmission Memory Switch

Address	Name	R/W	Default
530h	S_TXMEM_SW	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TXM_SW

Bit 0: TXM_SW

When this bit is set to 1, the banks of TX memory are switched.

In transmitting, after writing the TX memory, set this bit to 1.

Bit 0	Description
0	No operate
1	Switch the bank (Self clearing)

Receiving Memory Hold

Address	Name	R/W	Default
534h	S_RXMEM_HOLD	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RXM_HD

Bit 0: RXM_HD

During 1 of this bit, it is disabled to switch the banks of RX memory at receiving. In this situation, if receive the frame, the bank switching is not done until setting this bit to 0.

If RX memory is accessed immediately after receiving such as using interrupt, the timing conflict does not occurred. In this case, the bank hold is not necessary, set to 0.

Bit 0	Description
0	Enable bank switch
1	Bank hold

Communication State

Address	Name	R/W	Default
544h	S_STATE	R	0008h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Frame ID								-	-	-	-	State			

Bit [15:8]: Frame ID

Indicates the Frame ID in the received frame.

Bit [3:0]: State

Indicates the MNM1221 state.

Bit3	Bit2	Bit1	Bit0	State
1	0	0	0	INITIAL
0	1	0	0	CONFIG-A
0	0	1	0	CONFIG-B
0	0	0	1	RUNNING
Else				None

Over Number of Slave

Address	Name	R/W	Default
548h	S_OVER_N	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	OBS	ONS

Bit1: OBS (Over Block Sum)

In CONFIG-A state, when the sum of blocks is already over 32 previous to adding my node, this bit is set to 1.

	Description
0	Normal state
1	32 or more of blocks

Bit0: ONS (Over Node Sum)

In CONFIG-A state, when the sum of nodes is already over 32 previous to adding my node, this bit is set to 1.

	Description
0	Normal state
1	32 or more of nodes

Error Flags

Address	Name	R/W	Default
54Ch	S_ERR_FLAGS	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	Error Flags												

This register indicates various errors.

When an error is detected, each bit except Bit6 is latched to 1. After reading, it is cleared to 0.

For judgment of data error on the RX memory, this register is not used, but S_DCRC_ERR_L and S_DCRC_ERR_H are normally used.

Bit12: Frame length short

If the length of the frame is short, this bit becomes 1.

Bit11: Real-time frame CRC-error 2

If the Error Marking in the Real-time frame indicates an error, this bit becomes 1.

Bit10: Init-C frame CRC-error 2

Reserved (Always 0)

Bit9: Init-B frame CRC-error 2

If the Error Marking in the Init-B frame indicates an error, this bit becomes 1.

Bit8: Init-A frame CRC-error 2

If the Error Marking in the Init-A frame indicates an error, this bit becomes 1.

Bit7: MII RXER

If both RXER and RXDV of MII are “H”, this bit becomes 1.

Bit6: Real-time frame Data-CRC-error (OR of bits in S_DCRC_ERR register)

This bit is simply “OR” of all bits in both S_DCRC_ERR and S_DCRC_ERR_H,

so, not latched and not cleared after reading.

Bit5: Real-time frame CRC-error 1

If the Frame CRC in the Real-time frame indicates an error, this bit becomes 1.

Bit4: Init-C frame CRC-error 1

Reserved (Always 0)

Bit3: Init-B frame CRC-error 1

If the Frame CRC in the Init-B frame indicates an error, this bit becomes 1.

Bit2: Init-A frame CRC-error 1

If the Frame CRC in the Init-B frame indicates an error, this bit becomes 1.

Bit1: Timeout

In RUNNING state, if there is no frame within the setting time of S_TIMEOUT register, this bit becomes 1.

Bit0: Frame ID error

If the Frame ID in the frame indicates an error, this bit becomes 1.

Note:

When Bit12 or Bit0 is 1, MNM1221 does not output both XINTRX and XSYNC.

When Bit1 is 1, it does not output XSYNC. When S_INTRX_MSK is set to 1 additionally, it does not output XINTRX as well.

If reading this register in an interrupt by XINTRX or XSYNC, these bits indicate the previous error.

Data CRC Errors (L)

Address	Name	R/W	Default
550h	S_DCRC_ERR_L	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
#15	#14	#13	#12	#11	#10	#9	#8	#7	#6	#5	#4	#3	#2	#1	#0

Bit n: #n

When the Data CRC error is detected on the block in RUNNING state, this bit besomes 1. The bit number (#n) is in correspondence with the block number of RX memory.

For detection whether the data in RX memory is OK, use this register, and do not use S_ERR_FLAGS. Because there is a case “Though S_ERR_FLAGS indicates error, this register indicates OK.”, with error correcting function of MNM1221. When this register indicates OK, the data can be used.

	Description
0	Normal (OK)
1	CRC error (Cleared after read)

Data CRC Errors (H)

Address	Name	R/W	Default
554h	S_DCRC_ERR_H	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
#31	#30	#29	#28	#27	#26	#25	#24	#23	#22	#21	#20	#19	#18	#17	#16

Bit n: #n

The function is the same as S_DCRC_ERR_L register except the block number is different.

	Description
0	Normal state
1	CRC error (Cleared after read)

My Node Order

Address	Name	R/W	Default
558h	S_NODE_ORDER	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	My Node Order							

Bit [7:0]: My Node Order

Indicates the order of the cable connection for my node. This is detected in CONFIG-A state.

Value	Description
0	1st (beginning)
31	32nd

My Block Order

Address	Name	R/W	Default
55Ch	S_BLK_ORDER	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	My Block Order							

Bit [7:0]: My Block Order

Indicates the block number where my node data exists in the RX memory. This is detected in CONFIG-A state.

If plural blocks are occupied, the beginning number (smaller number) within the blocks is indicated.

Value	Description
0	Block #0
31	Block #31

Slave Node Sum

Address	Name	R/W	Default
560h	S_NODE_SUM	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	Slave Node Sum					

Bit [10:0]: Slave Node Sum

Indicates the sum of slave nodes. This is detected in CONFIG-B state.

Value	Description
1	1 of node sum
32	32 of node sum

Data Block Sum

Address	Name	R/W	Default
564h	S_BLK_SUM	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	Data Block Sum					

Bit [10:0]: Data Block Sum

Indicates the sum of slave data blocks. This is detected in CONFIG-B state.

Value	Description
1	1 of data blocks
32	32 of data blocks

MII Register Access

MNM1221 provides registers to access MII registers inside PHY chip.
In most PHY, this register access is not necessary since MNM1221 can perform properly with pin configuration only. But, some PHY such as KSZ8041 by Micrel needs the MII register setting as well. For the access, MDIO and MDC signals are used. See the following figure.

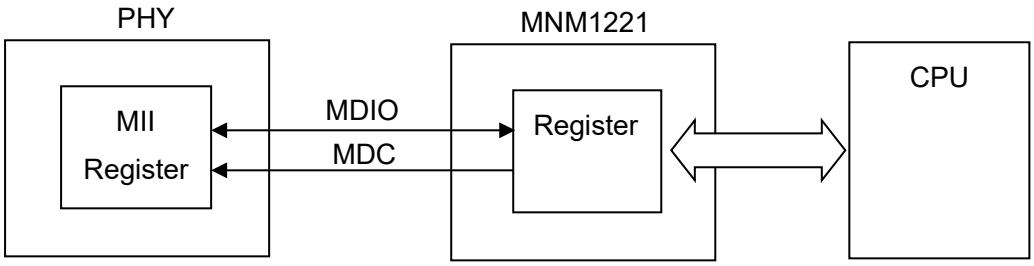


Table of Registers

(1) Control Registers

Address	Name	R/W	Default
520h	S_MDIO_WDAT	R/W	0000h
524h	S_MDIO_ADDR	R/W	0020h
528h	S_MDIO_WR	R/W	0000h
52Ch	S_MDIO_RD	R/W	0000h

(2) Status Register

Address	Name	R/W	Default
56Ch	S_MDIO_RDAT	R	0000h

MDIO Write Data

Address	Name	R/W	Default
520h	S_MDIO_WDAT	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write Data															

Bit [15:0]: Write Data

Set the data written into the MII register.

Note:

In the following time period, do not write any data into this register to perform proper operation.

- While S_MDIO_WR register shows 1 (in writing)
- 5 us after S_MDIO_WR register changed from 1 to 0
- While S_MDIO_RD register shows 1 (in reading)
- 5 us after S_MDIO_RD register changed from 1 to 0

MDIO Address

Address	Name	R/W	Default
524h	S_MDIO_ADDR	R/W	0020h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	PHY Address					Register Address				

Bit [9:5]: PHY Address

Set the address of PHY chip.

Bit [9:5]: Register Address

Set the address of MII register inside PHY chip.

Note:

In the following time period, do not write any data into this register to perform proper operation.

- While S_MDIO_WR register shows 1 (in writing)
- 5 us after S_MDIO_WR register changed from 1 to 0
- While S_MDIO_RD register shows 1 (in reading)
- 5 us after S_MDIO_RD register changed from 1 to 0

MDIO Write Command

Address	Name	R/W	Default
528h	S_MDIO_WR	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	WR

Bit 0: WR

When this bit is set to 1 after setting the S_MDIO_WDAT and S_MDIO_ADDR register, MII register writing will be started. After writing is completed, this bit returns to 0 automatically.

Bit 0	Description
0	Invalid
1	Writing (After writing, 0 cleared automatically)

Writing time for MII register: approximately 82 us

Note:

In the following time period, do not write any data into this register to perform proper operation.

- While S_MDIO_WR register shows 1 (in writing)
- 5 us after S_MDIO_WR register changed from 1 to 0
- While S_MDIO_RD register shows 1 (in reading)
- 5 us after S_MDIO_RD register changed from 1 to 0

MDIO Read Command

Address	Name	R/W	Default
52Ch	S_MDIO_RD	R/W	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RD

Bit 0: RD

When this bit is set to 1 after setting the S_MDIO_ADDR register, readout data from MII register will be stored to S_MDIO_RDAT register. After reading is completed, this bit returns to 0 automatically.

Bit 0	Description
0	Invalid
1	Reading (After reading, 0 cleared automatically)

Reading time for MII register: approximately 82 us

Note:

In the following time period, do not write any data into this register to perform proper operation.

- While S_MDIO_WR register shows 1 (in writing)
- 5 us after S_MDIO_WR register changed from 1 to 0
- While S_MDIO_RD register shows 1 (in reading)
- 5 us after S_MDIO_RD register changed from 1 to 0

MDIO Read Data

Address	Name	R/W	Default
56Ch	S_MDIO_RDAT	R	0000h

Bit fields:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Data															

Bit [15:0]: Read Data

Readout data from MII register is stored.

Note:
In the following time period, do not access this register to prevent invalid reading.

- While S_MDIO_WR register shows 1 (in writing)
- 5 us after S_MDIO_WR register changed from 1 to 0
- While S_MDIO_RD register shows 1 (in reading)
- 5 us after S_MDIO_RD register changed from 1 to 0

Chapter 4
Common to Master and Slave

Electrical Characteristics

Absolute Maximum Ratings

Symbol	Description	Condition	Value	Unit
V_{DD}	Supply Voltage		V_{SS}-0.5 to 4.0	V
V_I	Input Voltage *1	V_{DD}+0.5 < 4.0	V_{SS}-0.5 to V_{DD}+0.5	V
		D[31:0], A[10:0], XCS, XWR, XRD, XTXTIM, MODE[1:0], BUSMODE	V_{SS}-0.5 to 6.0	V
V_O	Output Voltage		V_{SS}-0.5 to V_{DD}+0.5	V
I_O	Output Current		+/- 14	mA
T_{STG}	Storage Temperature		-55 to +125	Degree C

*1: Voltage is defined on the basis of V_{SS}=GND=0.

Recommended Operating Conditions

Symbol	Description	Value			Unit
		Min	Typ	Max	
T_A	Operating Ambient Temperature	-40		+85	Degree C
V_{DD}	Operating Supply Voltage	3.0	3.3	3.6	V
f_{SCLK}	Clock Frequency OXTAL, IXTAL	24.999	25.000	25.001	MHz

DC Characteristics

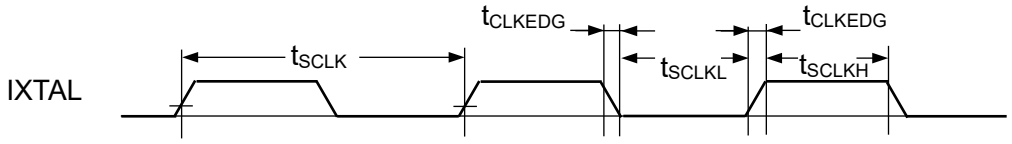
V_{DD} = 3.3V +/- 0.3V, V_{SS} = 0V, T_A = -40 to 85 degree C, unless otherwise specified

Symbol	Description	Conditions	Value			Unit
			Min	Typ	Max	
V_{IL}	Low Level Input Voltage		V_{SS}		V_{DD} x0.2	V
V_{IH}	High Level Input Voltage	D[31:0], A[10:0], XCS, XWR, XRD, XTXTIM, MODE[1:0], BUSMODE	V_{DD} x0.8		5.5	V
		Others	V_{DD} x0.8		V_{DD}+0.3	V
V_{OL}	Low Level Output Voltage	XLED/XWAIT: I_{OL} = 8mA	V_{SS}		0.4	V
		TDO: I_{OL} = 2mA				
		Others: I_{OL} = 4mA				
V_{OH}	High Level Output Voltage	XLED/XWAIT: I_{OH} = -8mA	V_{DD}-0.5		V_{DD}	V
		TDO: I_{OH} = -2mA				
		Others: I_{OH} = -4mA				
I_L	Input Leakage Current	V_I = 0V or V_{DD}	-5		5	uA
R_{PU}	Pull-up Resister	TRST, TCK, TMS, TDF: V_{IL} = 0V	25	50	200	k Ohm
R_{PD}	Pull-down Resister	MODE[1:0], BUSMODE: V_{IH} = V_{DD}	25	50	200	k Ohm
C_{PIN}	Pin Capacitance	T_A = 25 degree C			16	pF

Current Consumption	Max. 100 mA (For reference)

AC Characteristics

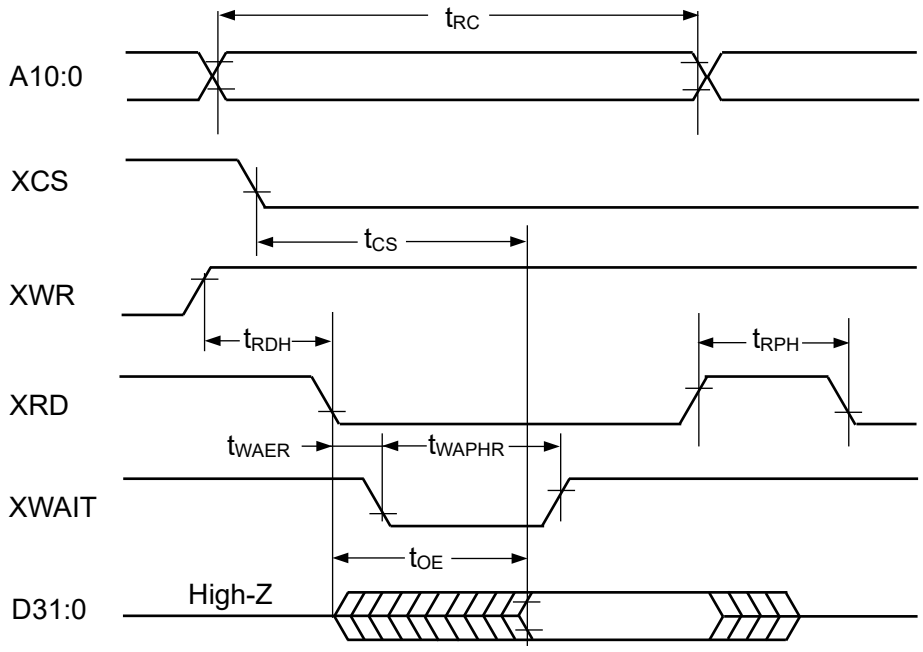
(1) Clock Input IXTAL



Symbol	Description	Value			Unit
		Min	Typ	Max	
t_{SCLK}	Clock frequency of IXTAL (Accuracy +/- 50ppm)	39.998	40	40.002	ns
t_{SCLKL}	IXTAL low	14	20	26	ns
t_{SCLKH}	IXTAL high	14	20	26	ns
$t_{CLKEDGE}$	IXTAL rising and falling time			4	ns

Note:
- The same oscillator clock as driving PHY chip must be inputted.

(2) Read Access Timing

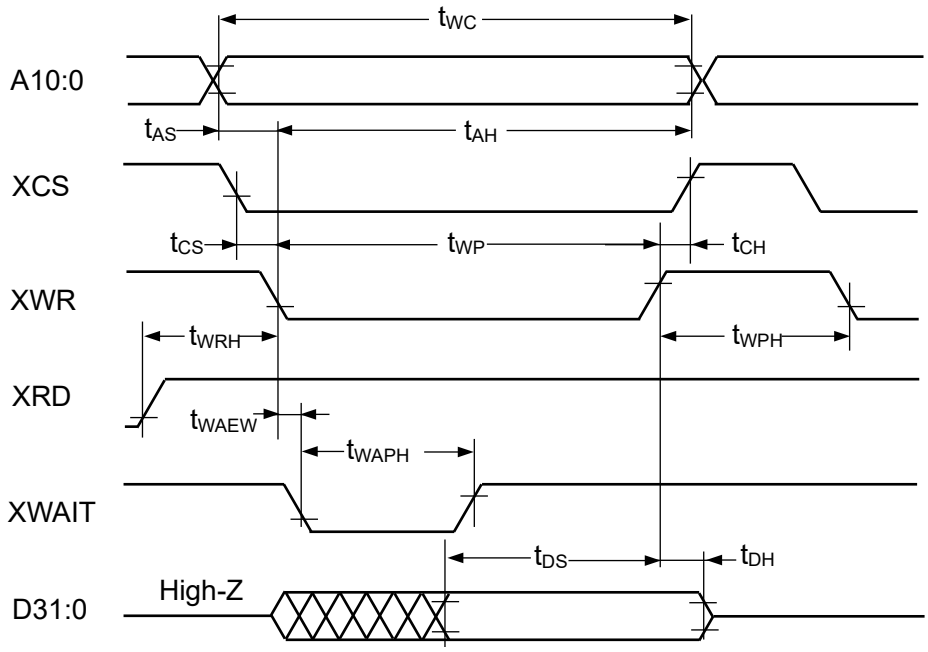


Symbol	Description	Value			Unit
		Min	Typ	Max	
t_{RC}	Read cycle time.	240			ns
t_{CS}	Chip select setup time is the delay from stable addresses and stable XCS to valid data at the output pins.			180	ns
t_{RDH}	Read pulse hold time	45			ns
t_{RPH}	Read pulse width high	45			ns
t_{OE}	Output enable time is the delay from the falling edge of XRD to valid data at the output pins (Assuming the addresses have been stable for at least t_{RC}-t_{CS} time).			180	ns
t_{WAER}	Wait enable time is the delay from the falling edge of XRD to valid XWAIT at the read mode			25	ns
t_{WAPHR}	Wait pulse width high at the read mode	140		200	ns

Notes:

- To ensure access, XWAIT should be connected to a WAIT input of CPU.
  When both XCS and XRD are Low, XWAIT becomes Low. And, after MNM1221 outputs valid data, it returns to High.
- When using fast CPU, special care of t_{RDH} and t_{RPH} should be taken.

(3) Write Access Timing

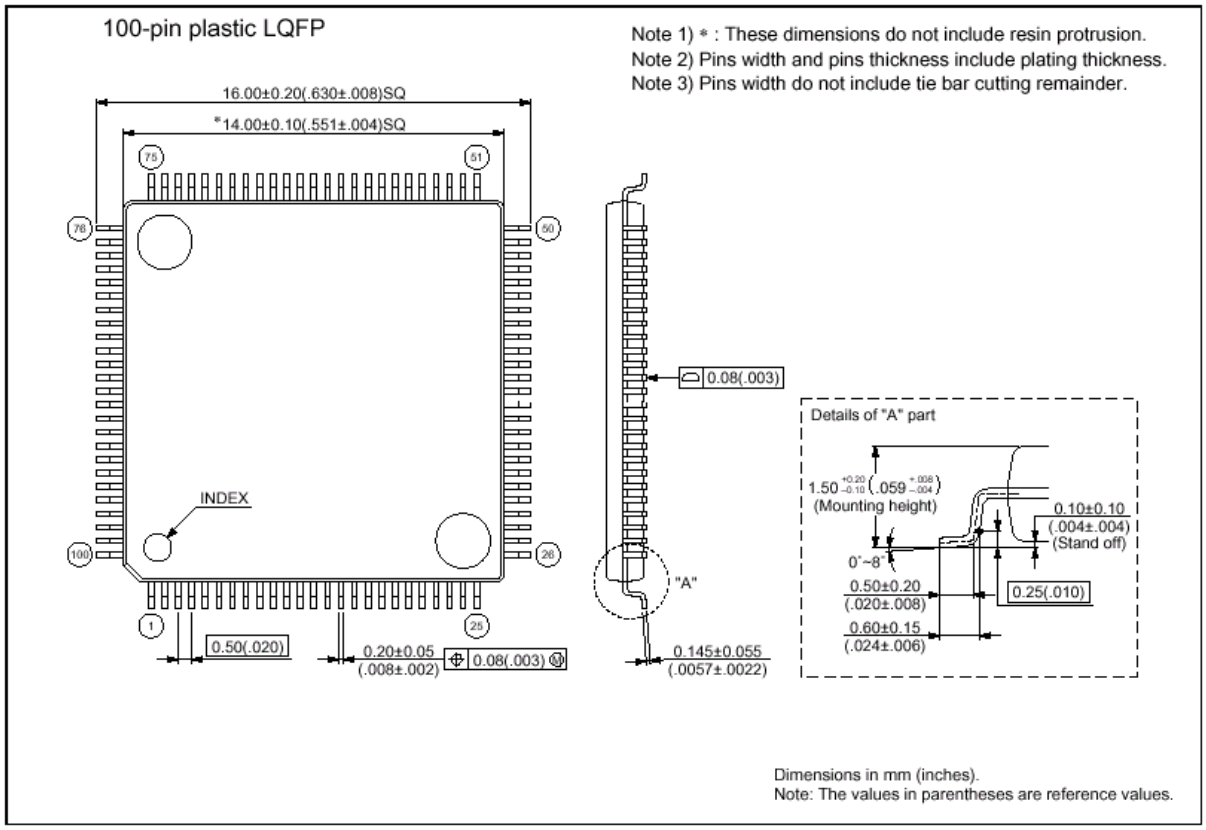


Symbol	Description	Value			Unit
		Min	Typ	Max	
t_{WC}	Write cycle time.	120			ns
t_{AS}	Address setup time.	0			ns
t_{CS}	Chip select setup time	0			ns
t_{AH}	Address hold time	120			ns
t_{CH}	Chip select hold time.	0			ns
t_{WP}	Write pulse width	120			ns
t_{WRH}	Write pulse hold time	45			ns
t_{WPH}	Write pulse width high	45			ns
t_{DS}	Data setup time	45			ns
t_{DH}	Data hold time	0			ns
t_{WAEW}	Wait enable time is the delay from the falling edge of XWR to valid XWAIT at the write mode			25	ns
t_{WAPHW}	Wait pulse width high at the write mode	60		120	ns

Notes:

- To ensure access, XWAIT should be connected to a WAIT input of CPU.
  When both XCS and XWR are Low, XWAIT becomes Low. And, after the data setup time of MNM1221 is secured, it returns to High.
- When using fast CPU, special care of t_{WRH} and t_{WPH} should be taken.

Dimensions



Soldering Information

Reflow condition:

	Temperature
Peak	260 deg C maximum
10 s or shorter	255 deg C

Note:

The package is in compliance with Pb-Free.

Ordering Information

Ordering No.	DV0P444-9
Packing Quantities	90 pcs